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# Update on Readout Electronics: An End-to-End Demonstrator

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EUROPEAN SPALLATION SOURCE

# Data Acquisition Electronics - I.K.C.

Collaborative partnership between

Science & Technology Facilities Council

EUROPEAN SPALLATION SOURCE

Daresbury


Detector Group Richard Hall-Wilton

EUROPEAN SPALLATION SOURCE

RAL, Technology Group, Marcus French

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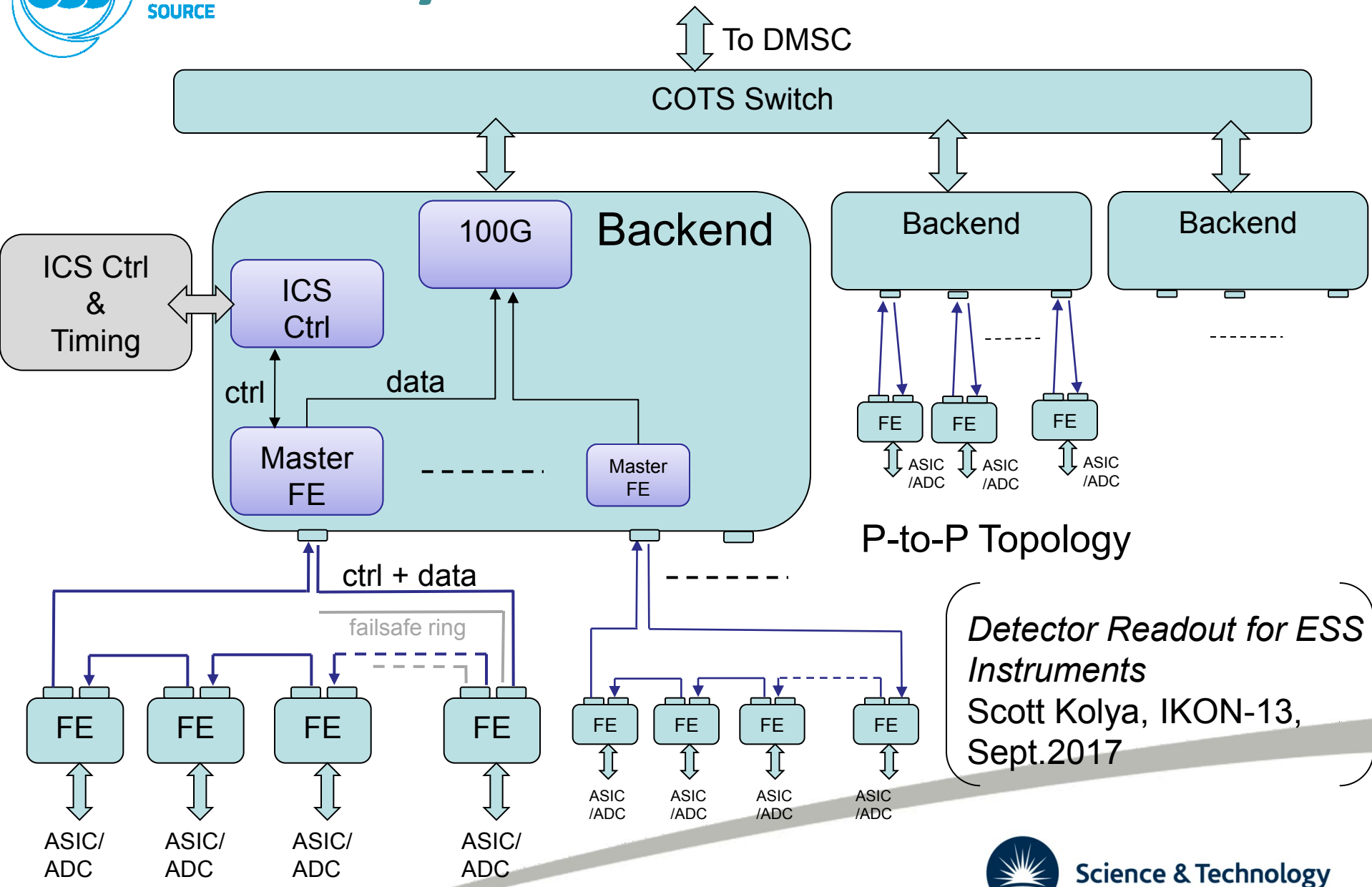
# System Architecture




*Detector Readout for ESS Instruments*
Scott Kolya, IKON-13, Sept.2017

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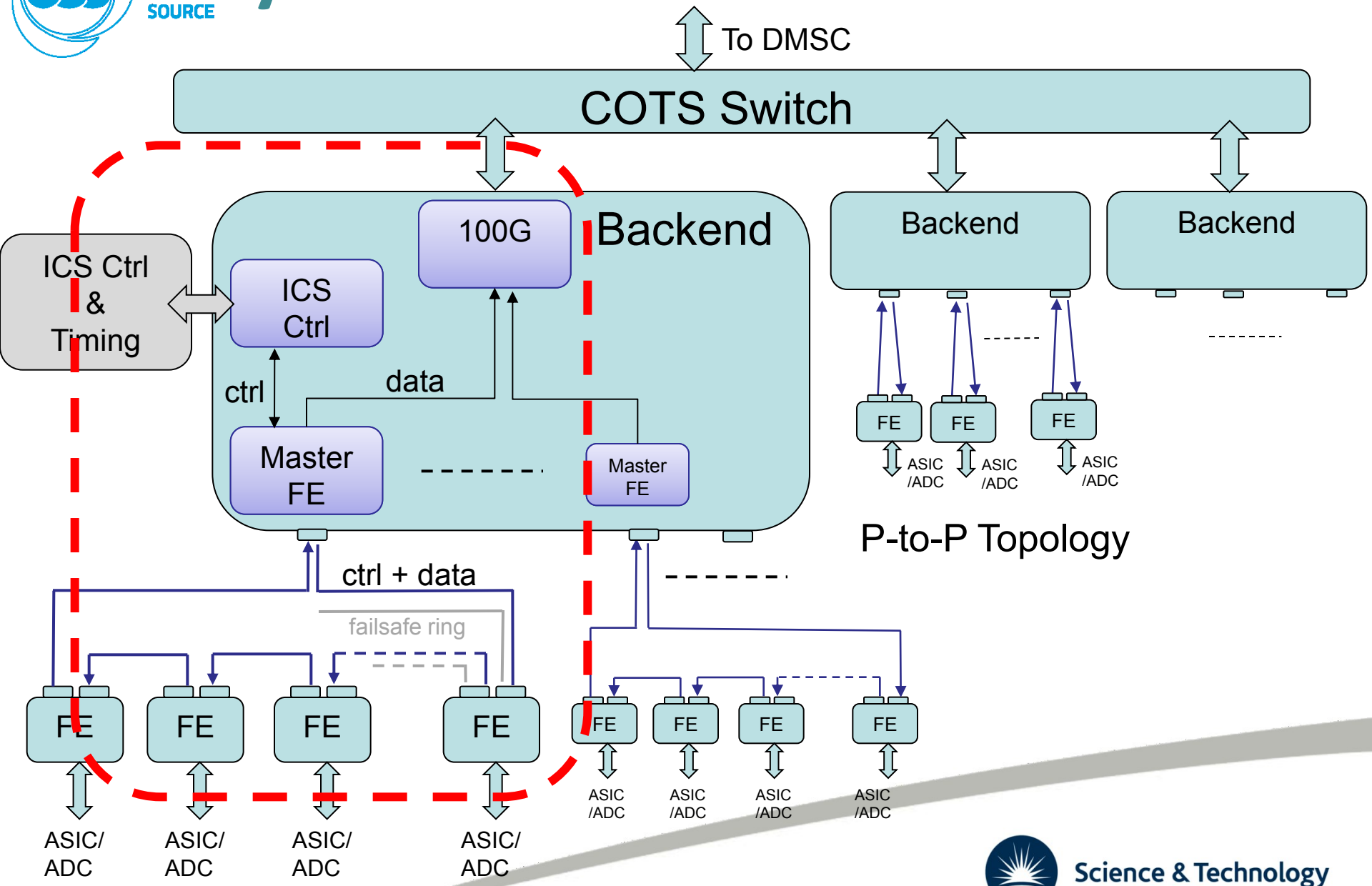
# Today : An End-to-End Demonstrator

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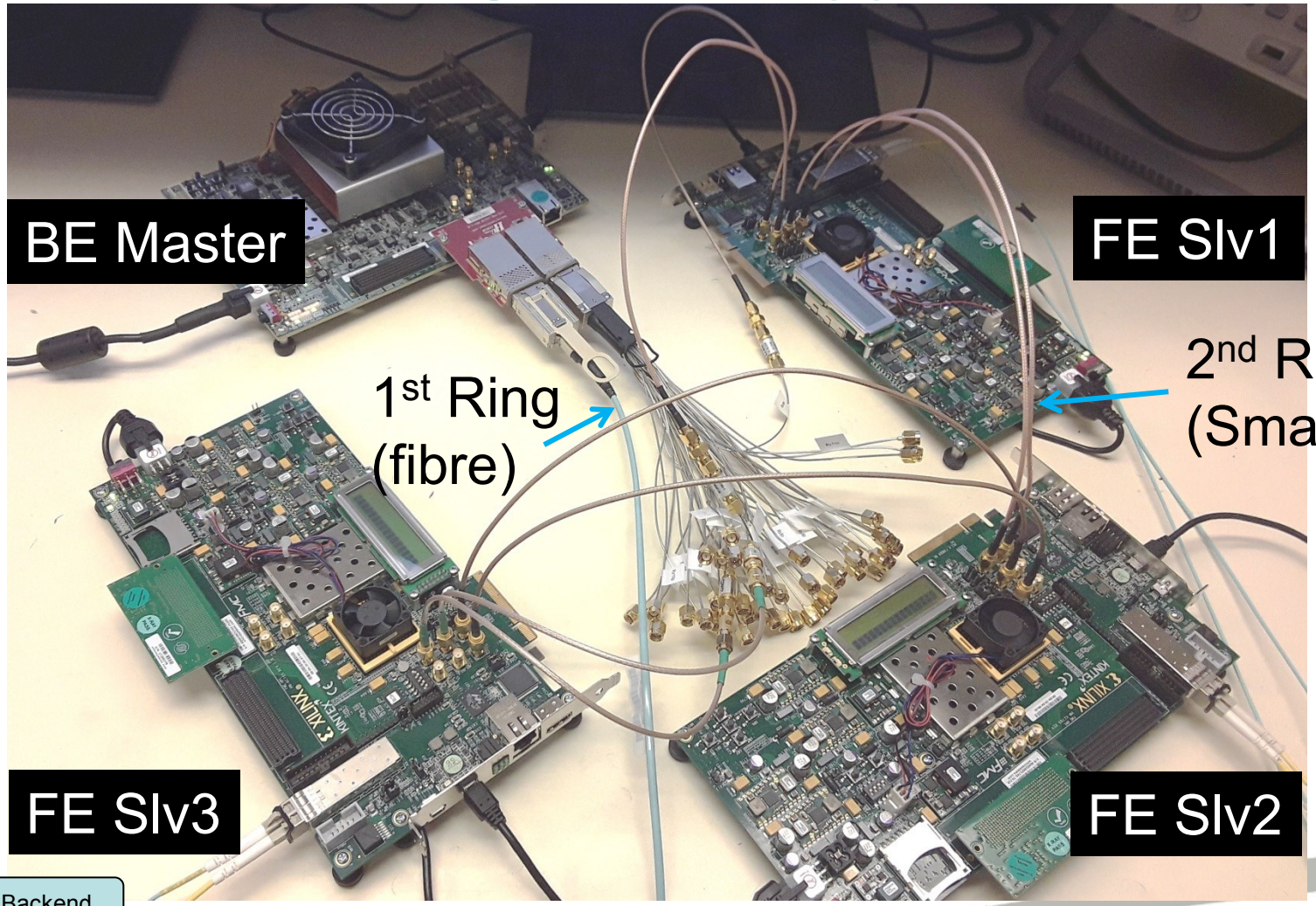
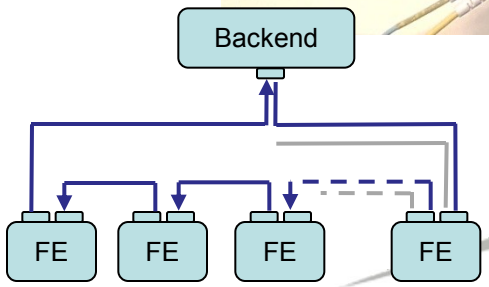
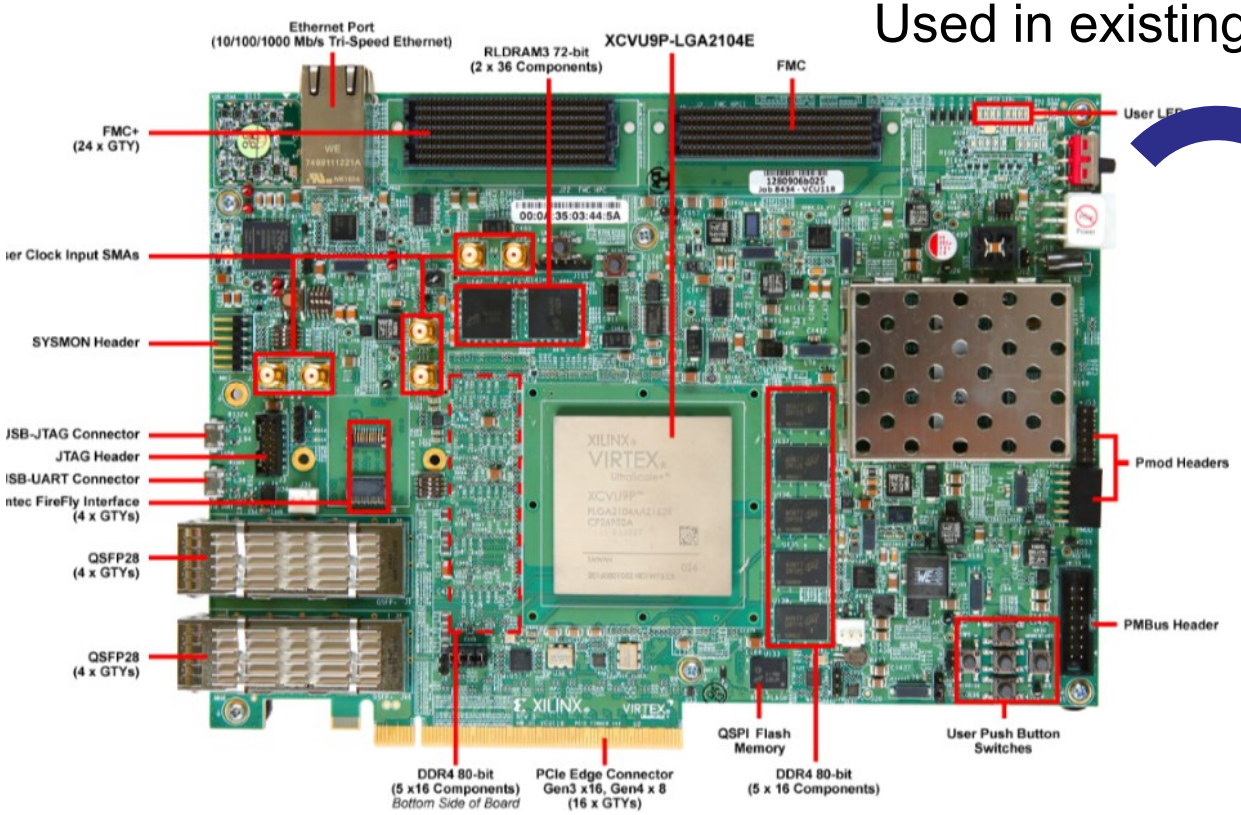
# Ring Prototype



# Backend Hardware




Used in existing ESS BE demonstrator


- Xilinx VCU118
- Virtex, Ultrascale+

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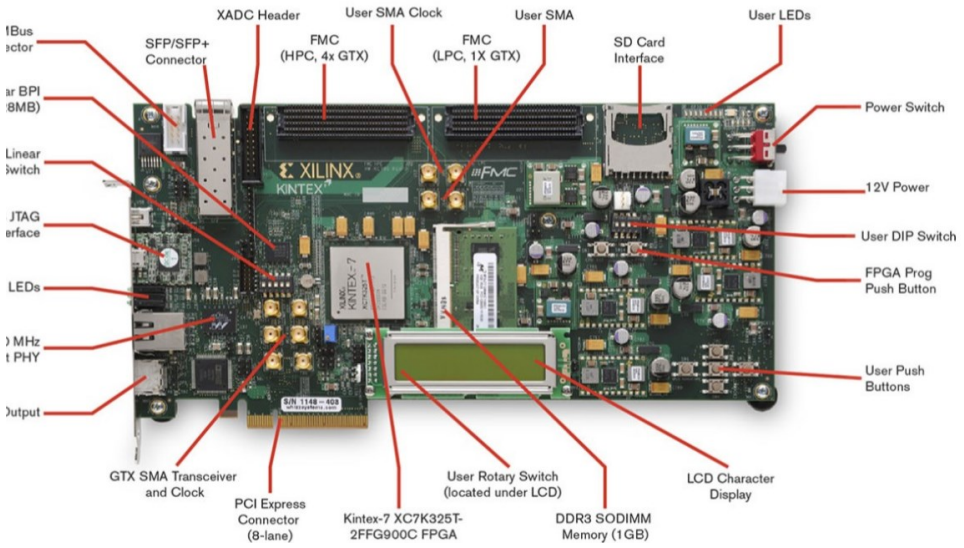
# FE Hardware

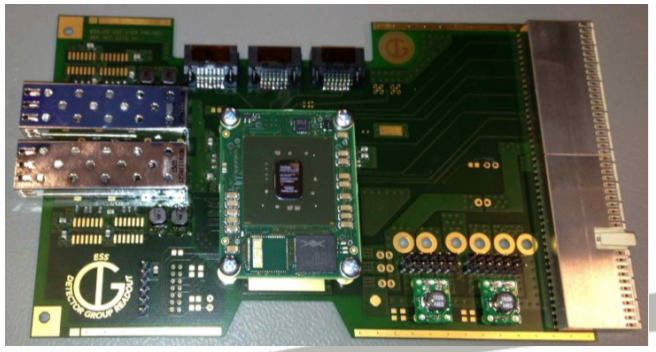
Current prototyping platform:

- Xilinx KC705
- Kintex, 7-series




Next stage:

- Move to custom platform.





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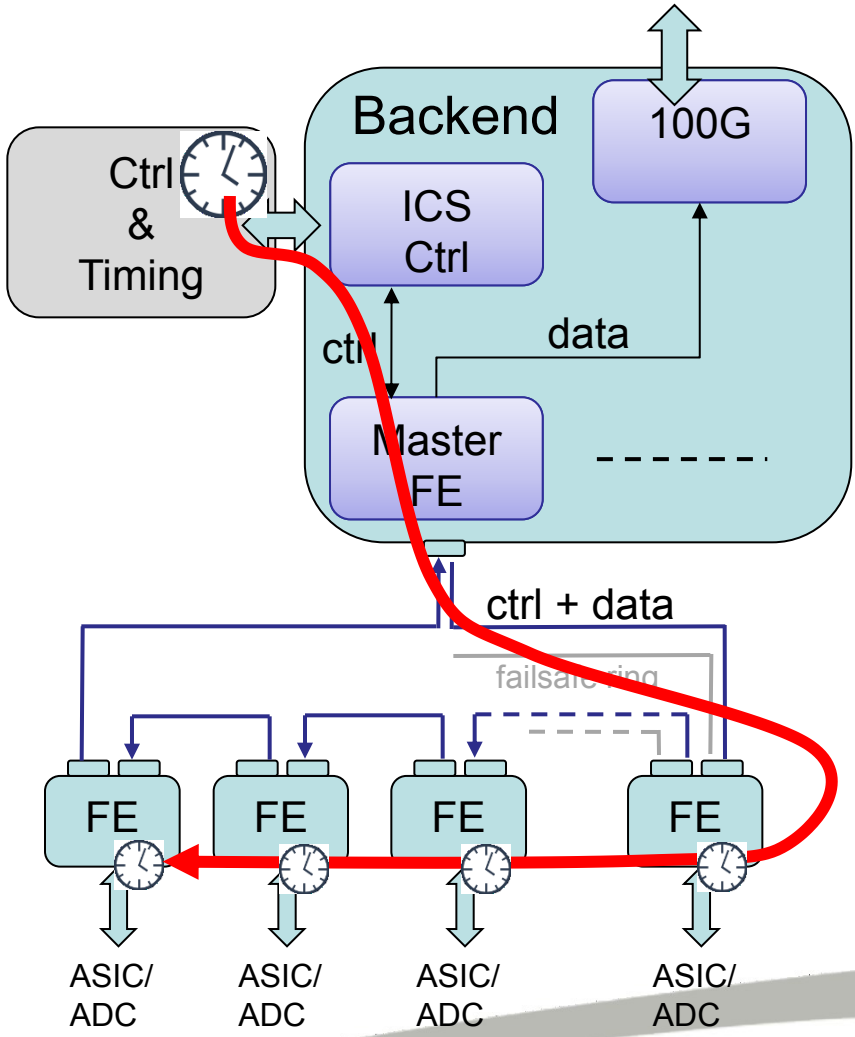
# Front End Functions

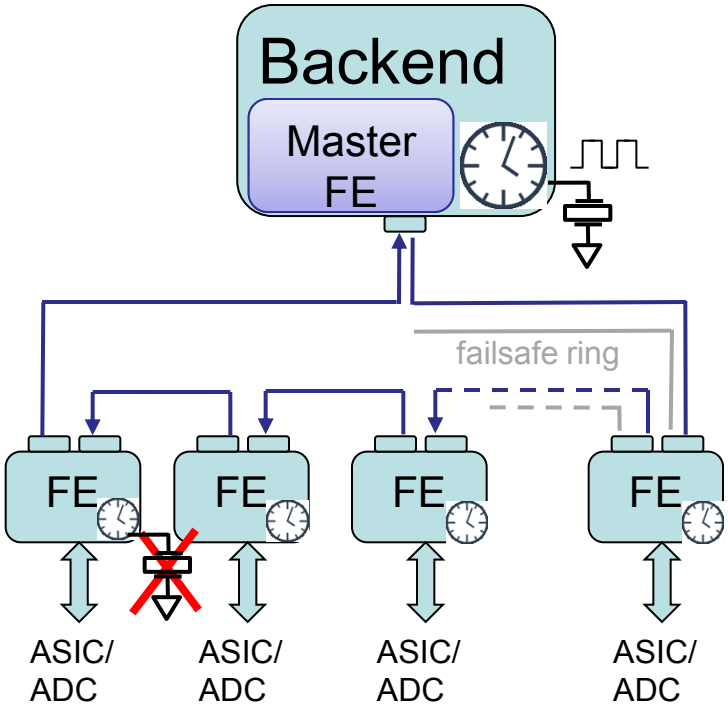
- Acquire accurate timestamp.
- Collect digitized (timestamped) neutron data, and downstream it to the BE.
- Receive & Return Slow Control data (e.g. ADC-register W/R's)



# Timestamp Challenges

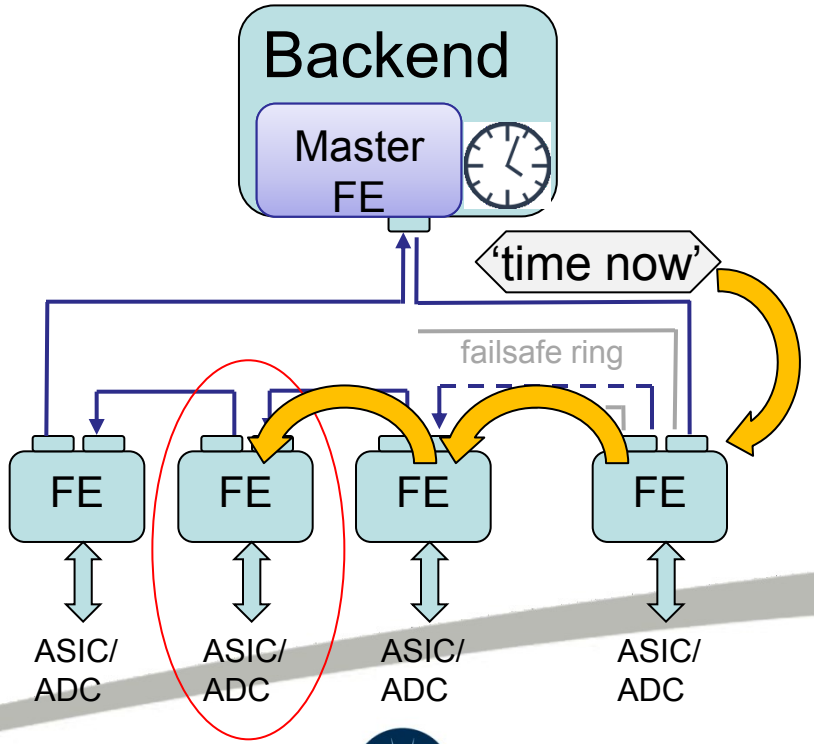
## Clock Synchronisation

Separate FPGAs must be clocked synchronously for local timestamps to 'tick' equally.




## Timestamp Distribution

Master must allow for transit delays when initialising FE's.

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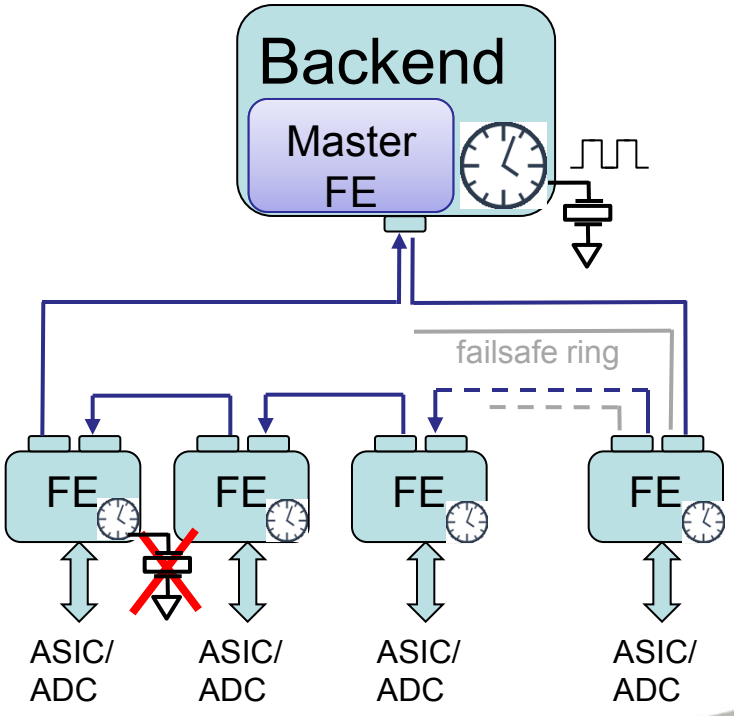
# Clock Synchronisation

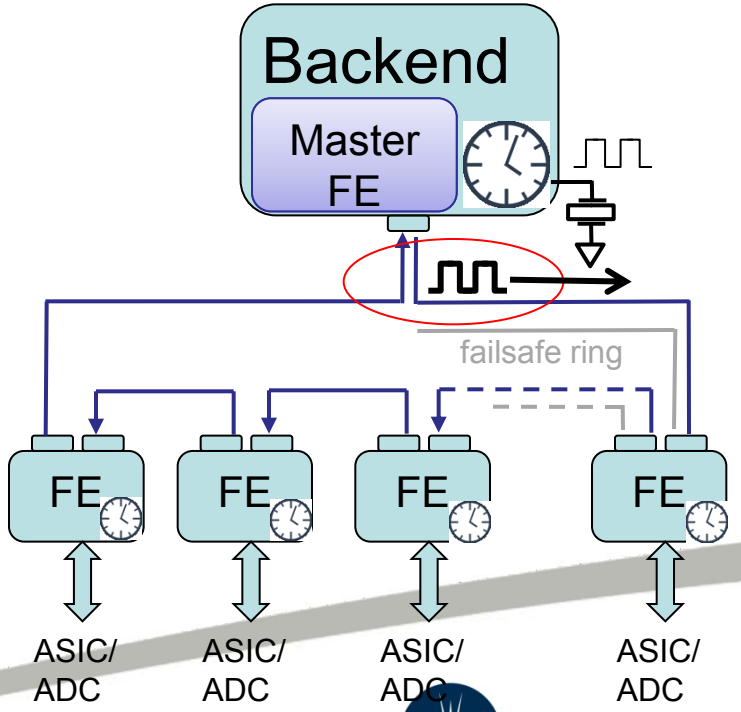
## Challenge

Local timestamps must be clocked (‘tick’) synchronously

## Solution

Master embeds its clock as 8b10b bitstream. Each slave recovers and re-transmits the clock.

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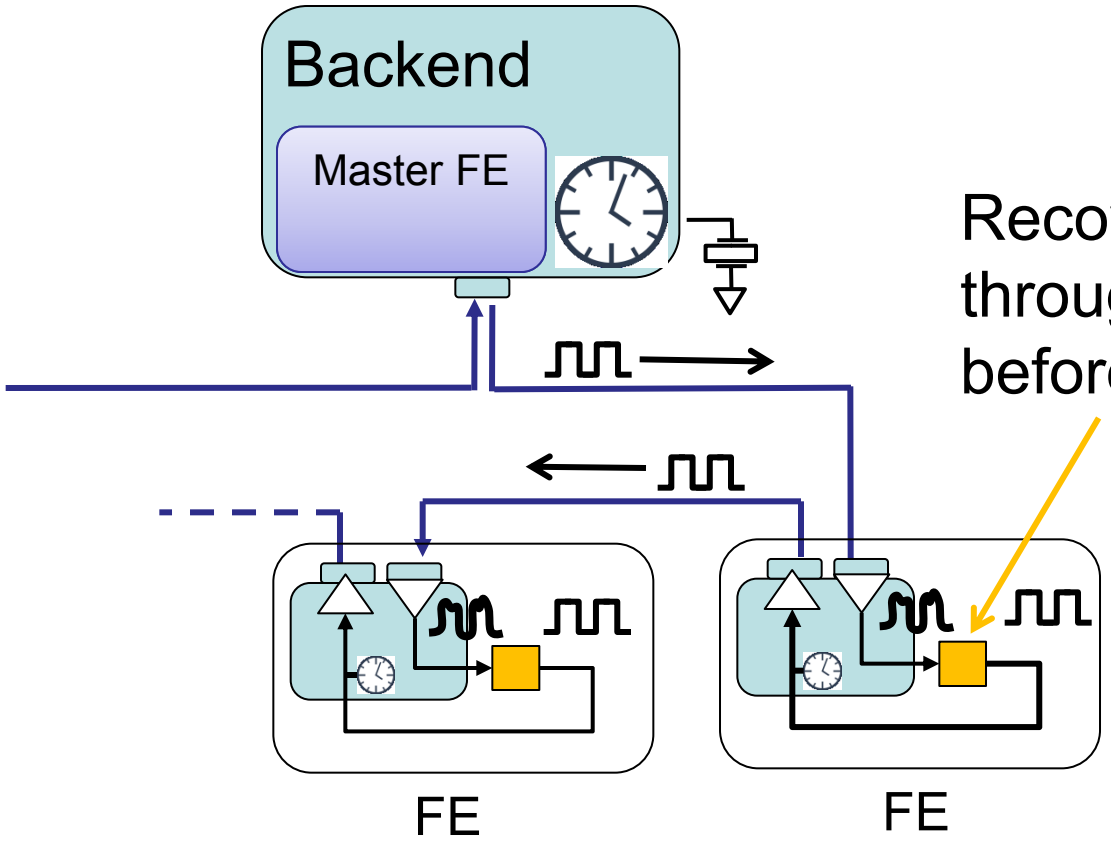
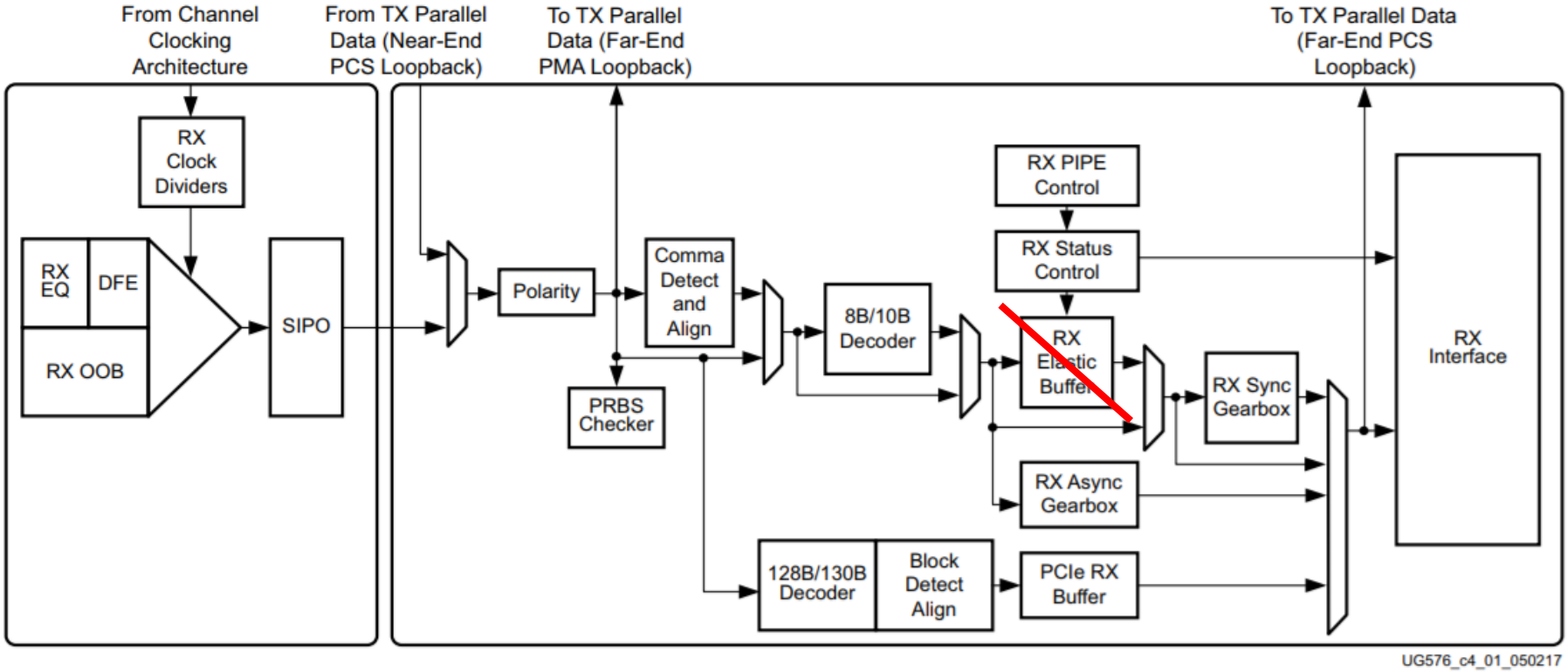
# Clock Synchronisation




Recovered clock is sent through jitter-cleaner IC before forwarding

# Clock Synchronisation

Deterministic clock recovery requires that (normally present) Elastic Buffers in FE Slave transceivers are disabled.



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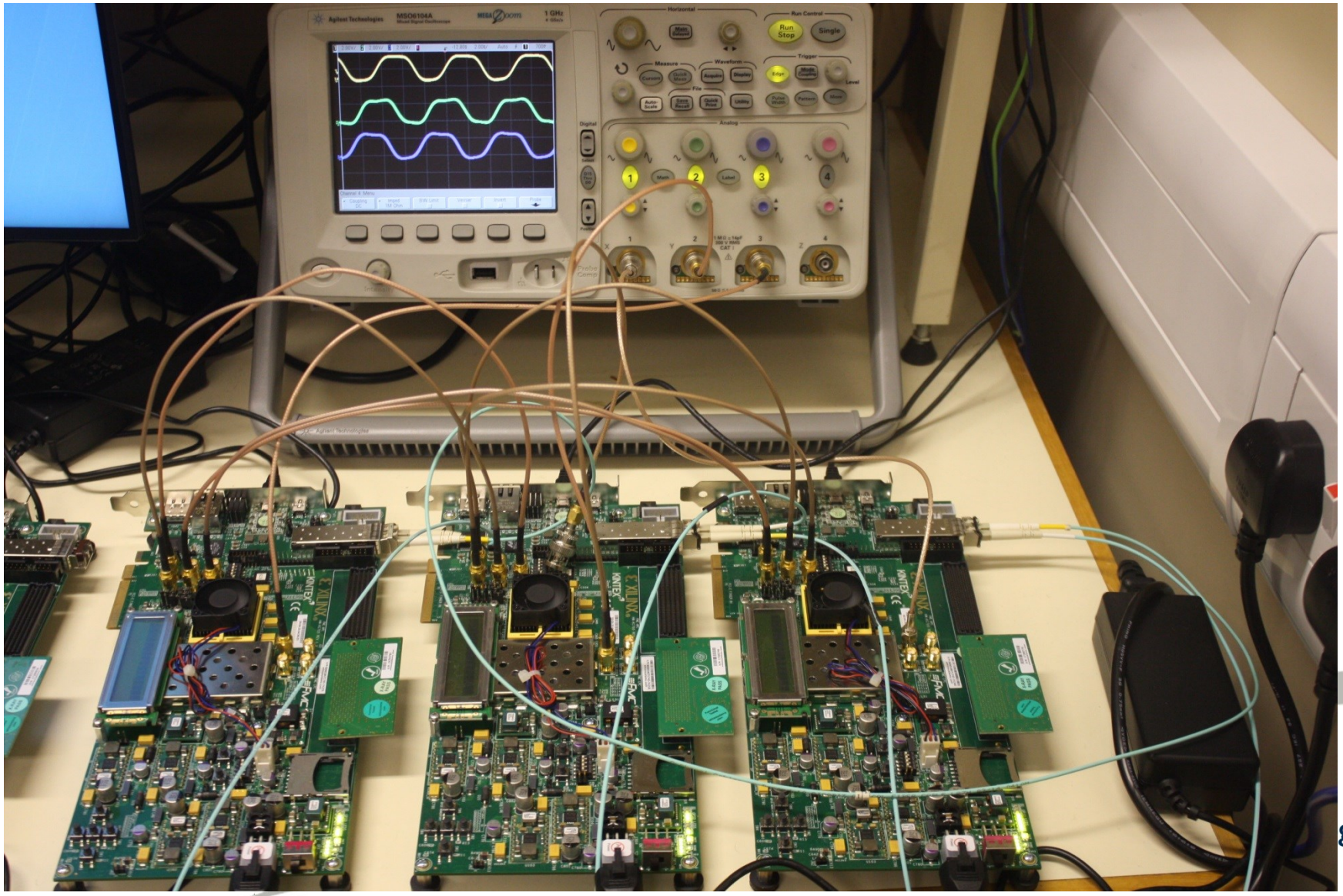
# Clock Synchronisation - Result

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# Challenge2 – Timestamp Distribution

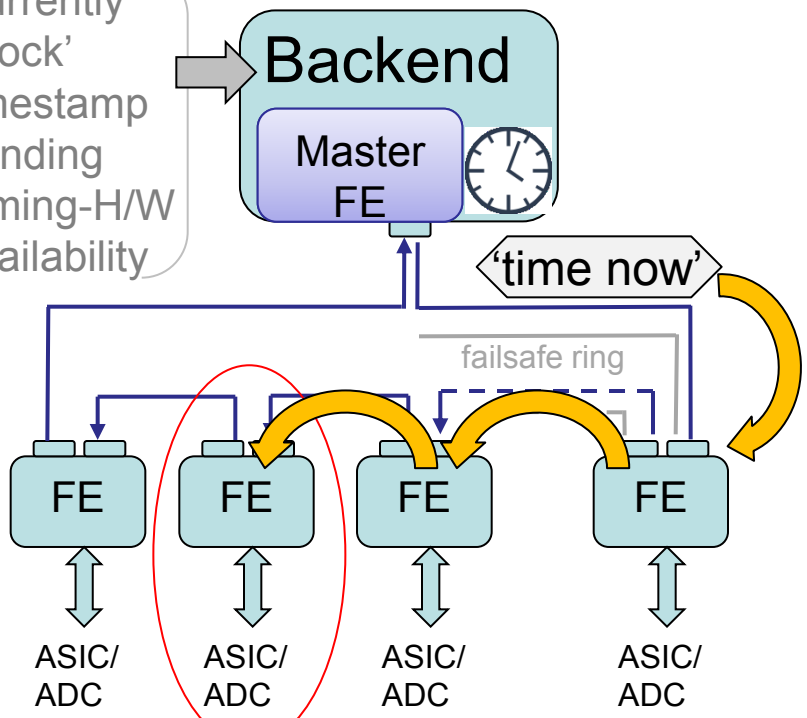
## Challenge

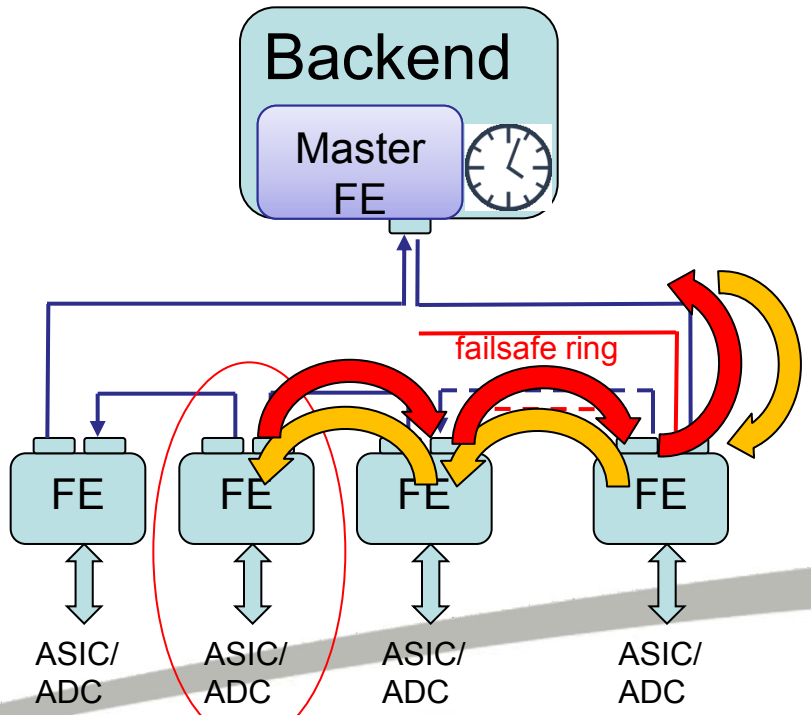
Master must allow for transit delays when initialising FE's.

## Solution

Use second ring to measure transit delays.

Currently 'mock' timestamp pending Timing-H/W availability

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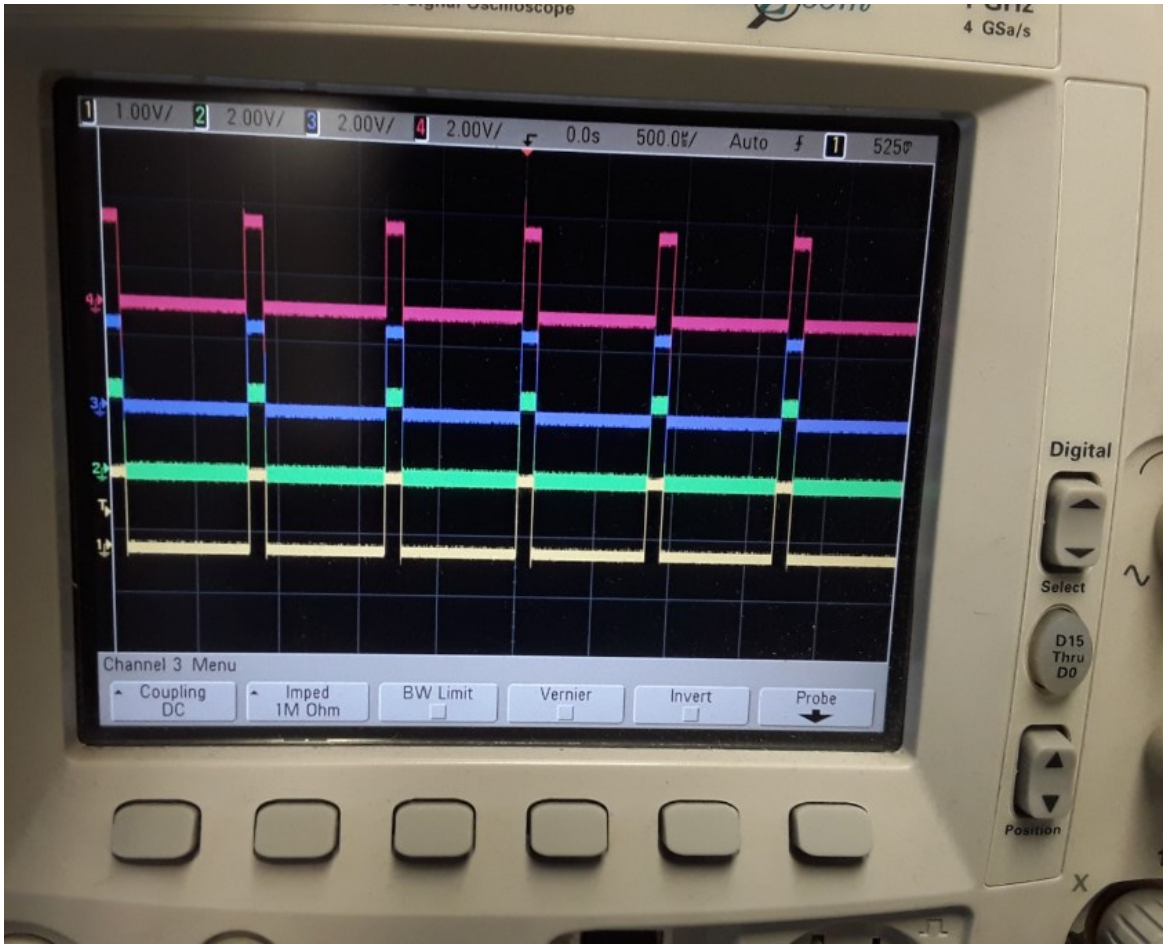
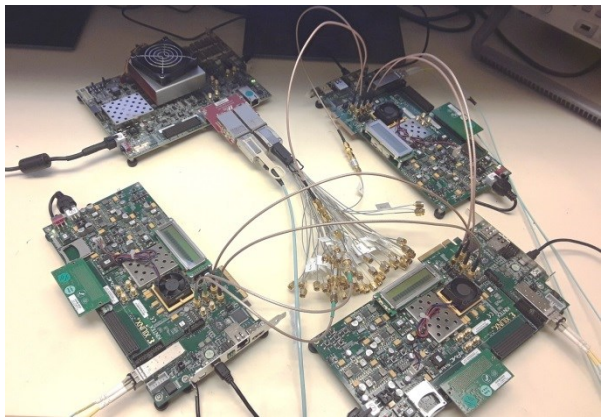
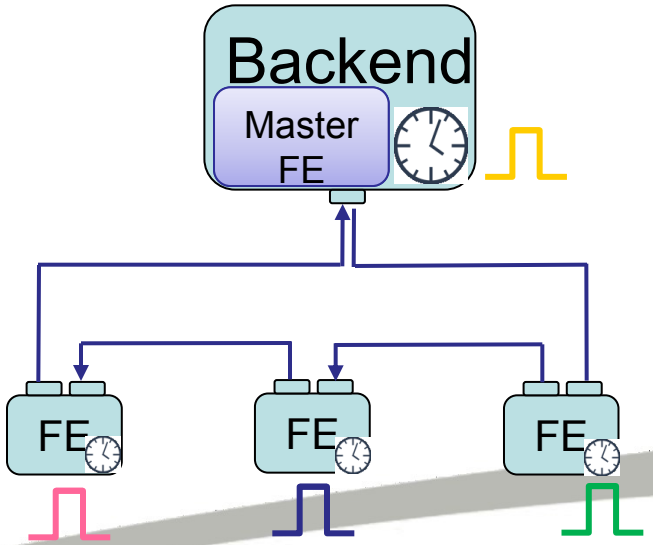
# Timestamp Synchronisation – Result






Based on local timestamp, FE's emit a pulse-per-millisec

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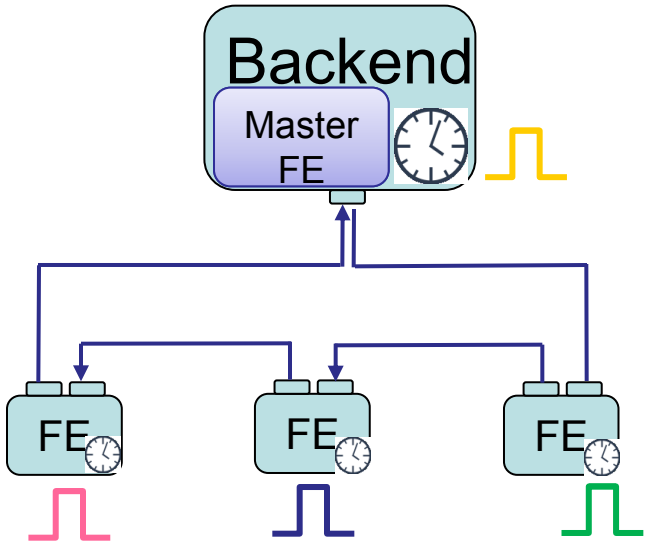
# Timestamp Synchronisation (detail)

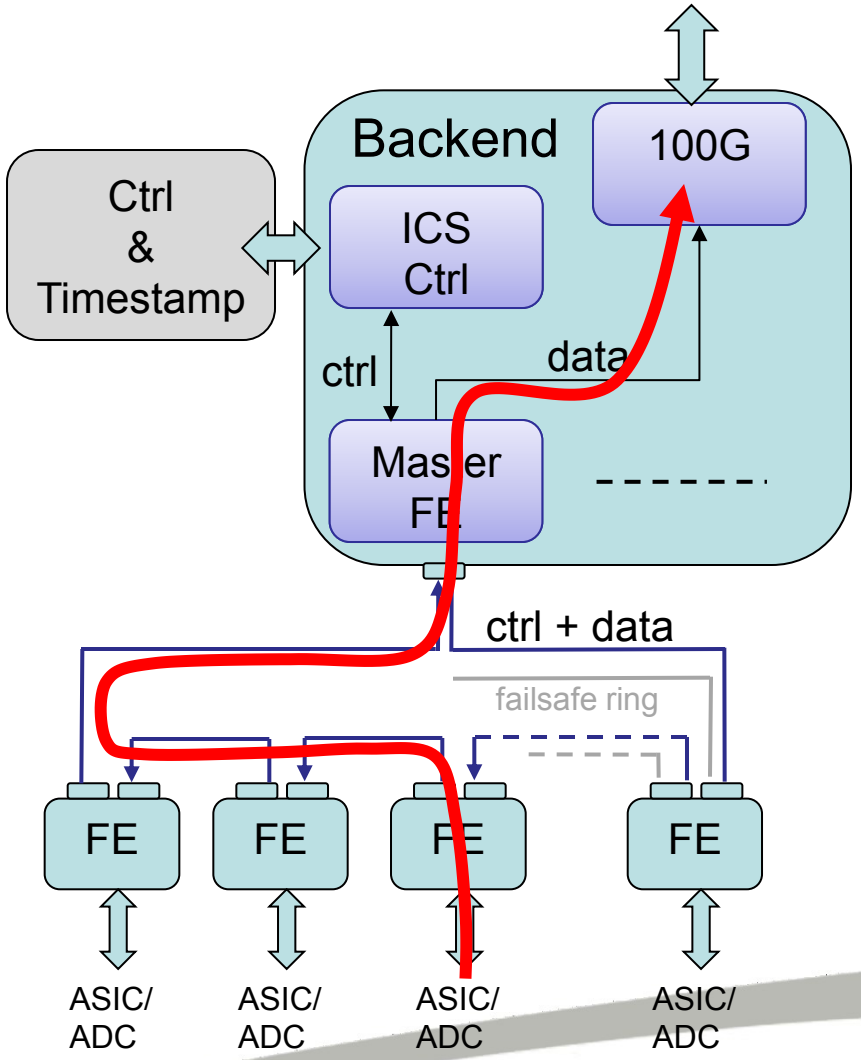
Stable, Δt ~ 10ns,  timestamp synchronisation*

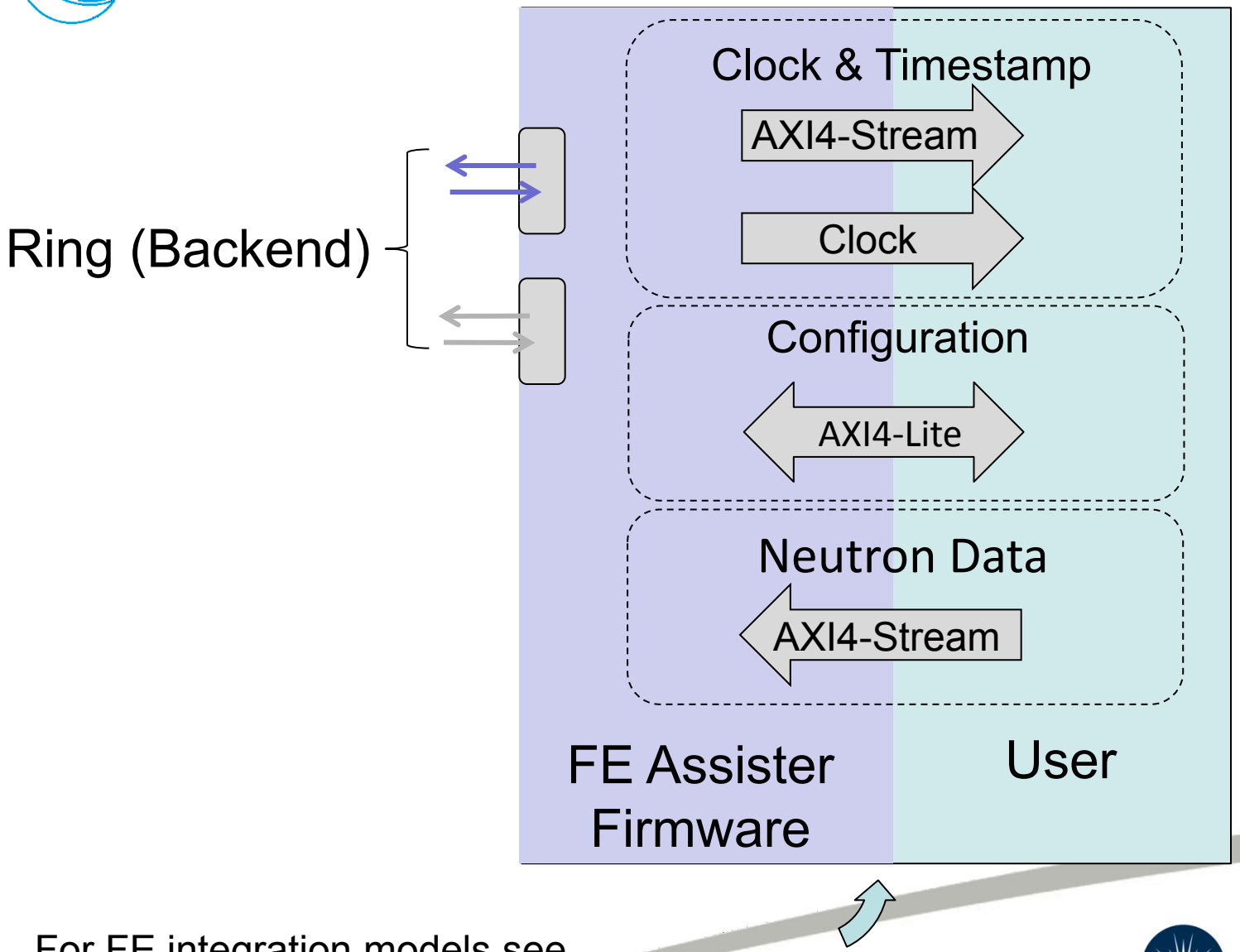

(* c.f Δt = 11.357ns requirement,
Gahl et al. *Hardware Aspects, Modularity and Integration of an Event Mode Data Acquisition and Instrument Control for the European Spallation Source (ESS)*, 2014, arXiv: 1507.01838v1)

# Front End Functions

- Acquire accurate timestamp.
- Collect digitized (timestamped) neutron data, and downstream it to the BE.
- Receive & Return Slow Control data (e.g. ADC-register W/R's)



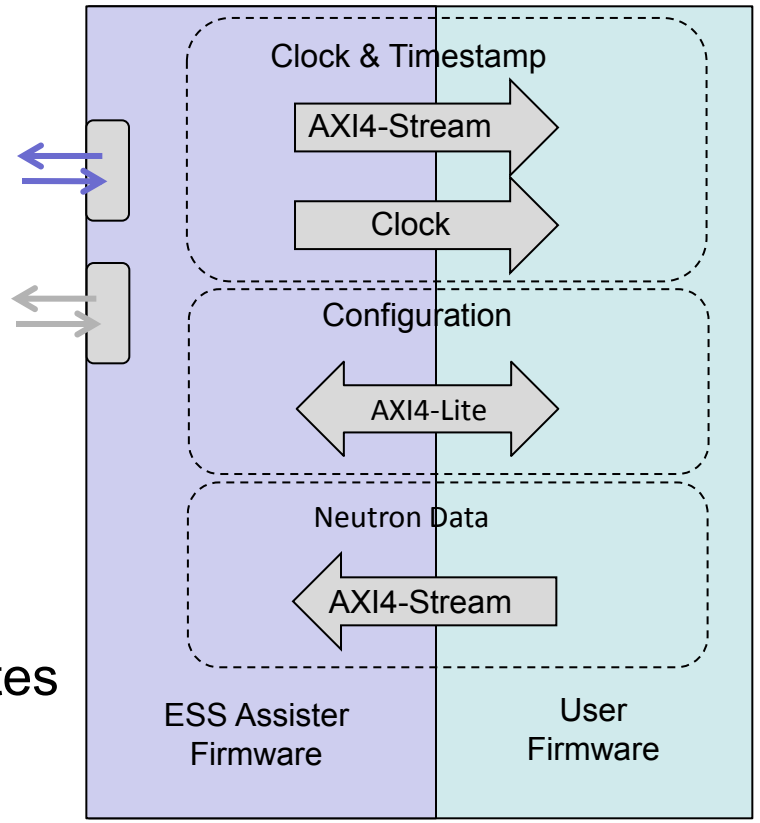
# Front End User Interface



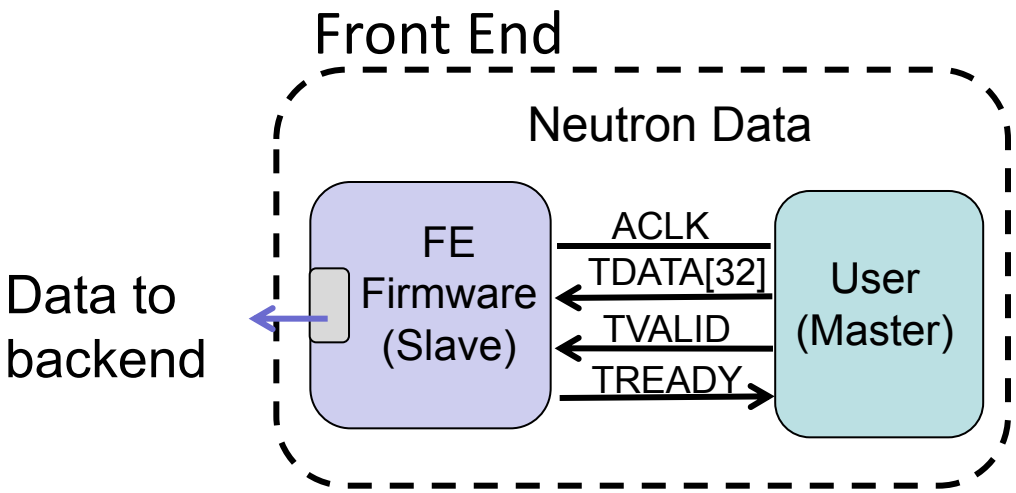

For FE integration models see BrightnESS Deliverable Report: D4.1 – *Integration Plan for Detector Readout*, Scott Kolya et.al. 2017

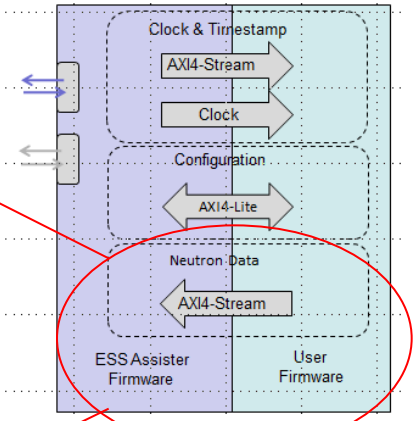
# AXI Interface To Users

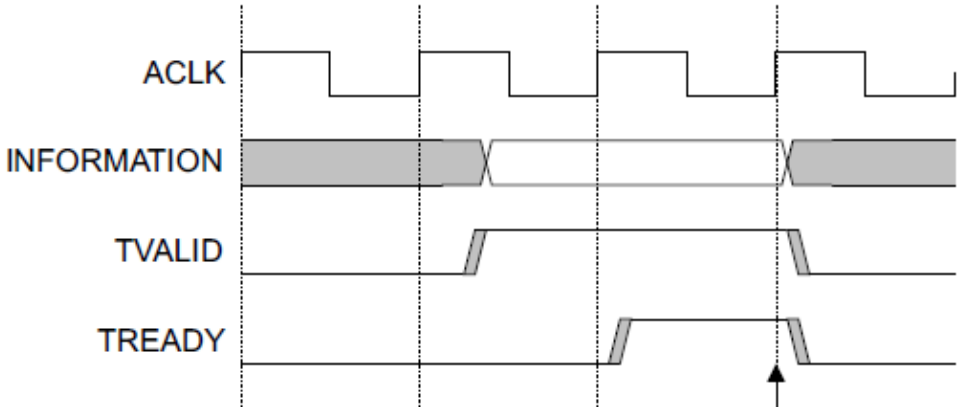
- Originated by Arm Ltd.
- Free documentation
- Extensive support from FPGA-vendors (Xilinx).
- Various ‘flavours’
  - AXI4-Stream - Simple Data Exchange
  - AXI4-Lite - Address based Read/Writes
  - AXI4 - ‘Heavyweight’ e.g. burst transfers etc.



# Neutron Data AXI4-Stream I/f

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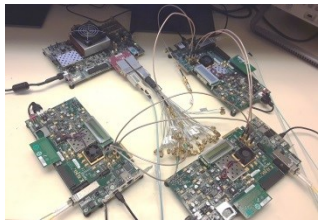
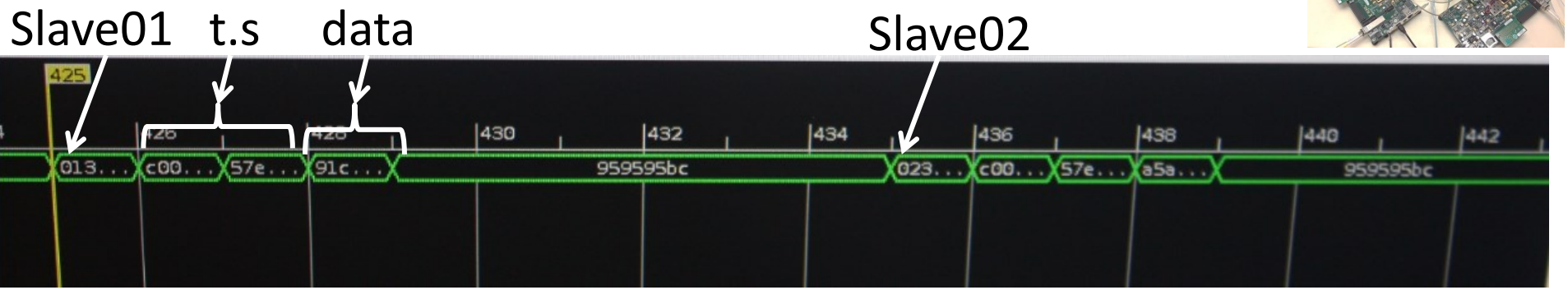
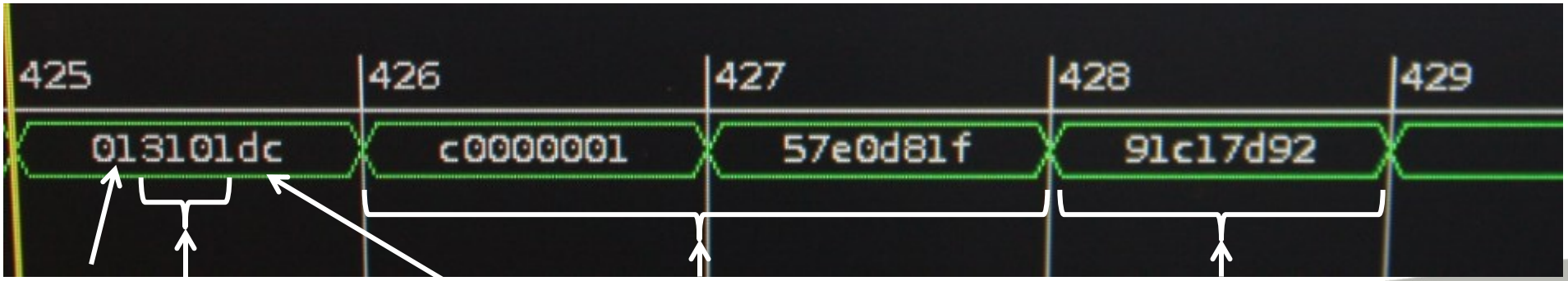
# Collecting Data - Result



A) Screenshots of data packets returning to FE Master.




B) Detail:




Slave i.d.

slave status incl. fifo level

packet type (data / control)

64-bit timestamp

32-bit Data

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21

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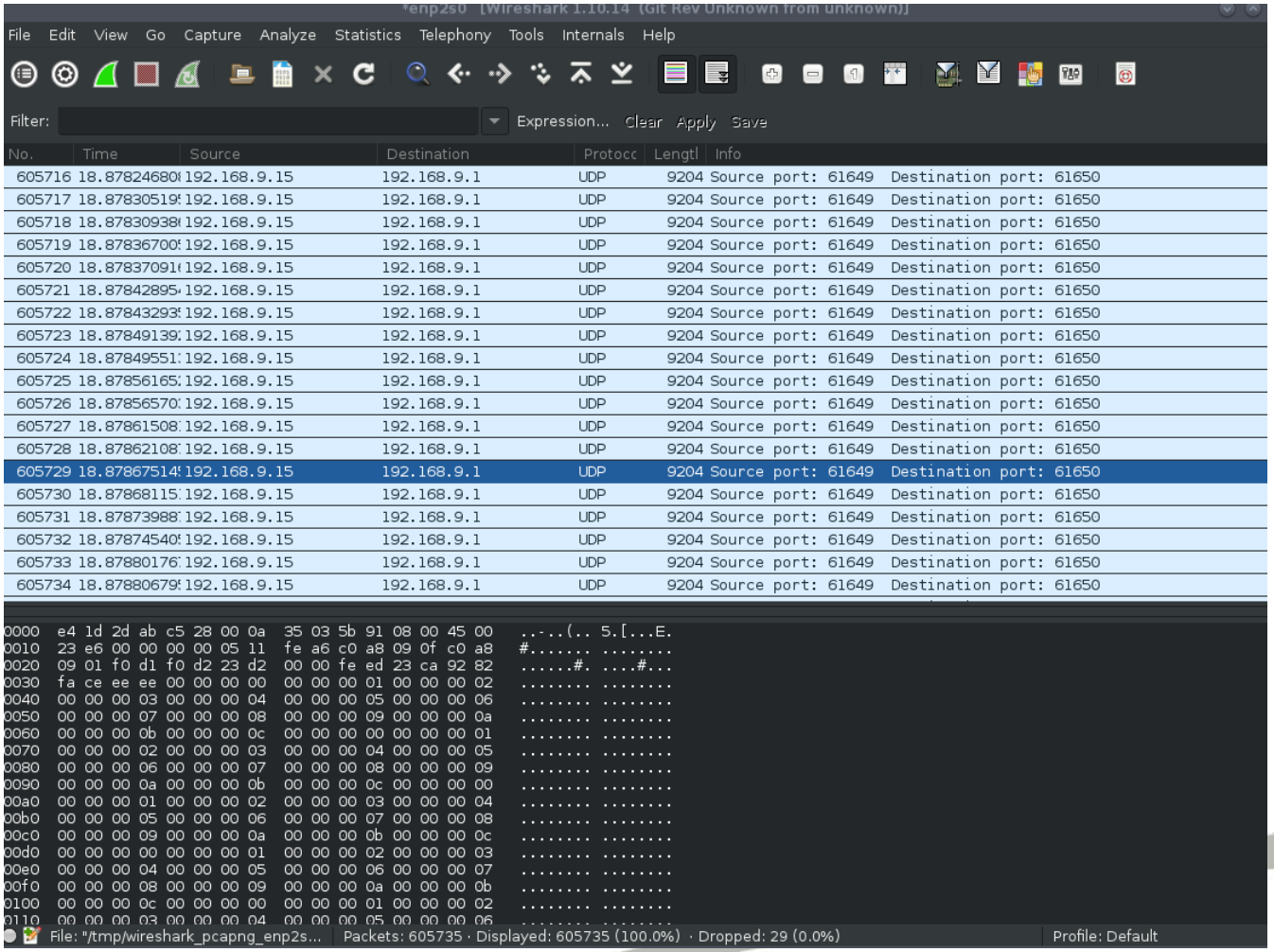
# 100G Data Packets

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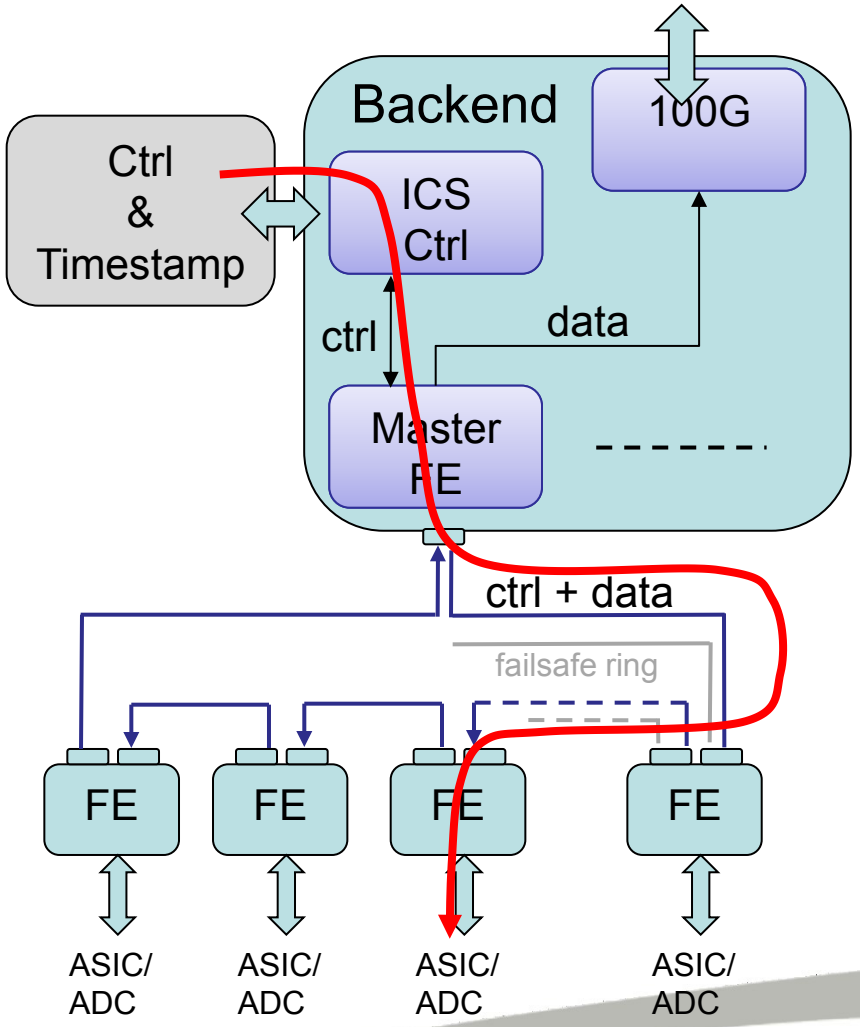
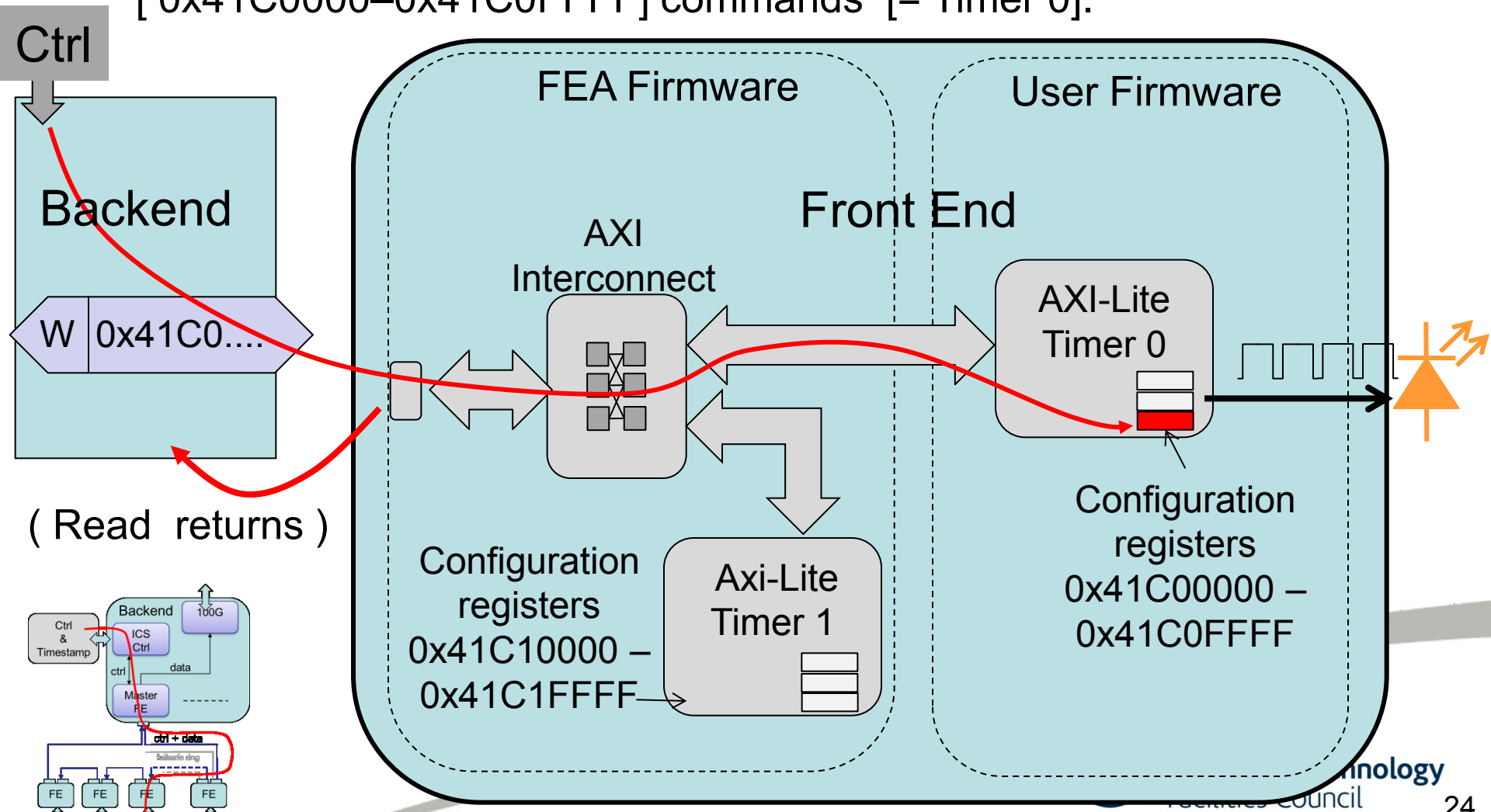
# Front End (FE) Functions

- Acquire accurate timestamp.
- Collect digitized (timestamped) neutron data, and downstream it to the BE.
- Receive & Return Control data (e.g. ADC-register W/R's)

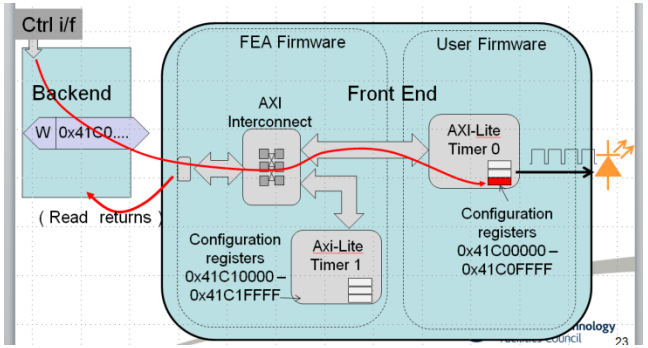


# Memory-mapped Slow Control – Example:

Backend launches packets onto ring containing “write-to-memory” [ 0x41C0000–0x41C0FFFF] commands [= Timer 0].

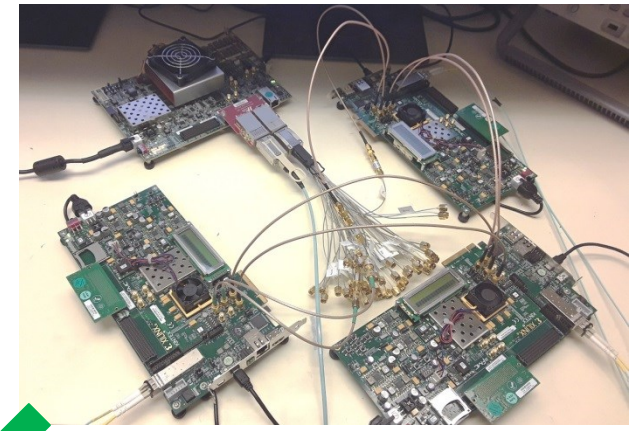


# Memory-mapped Slow Control Example

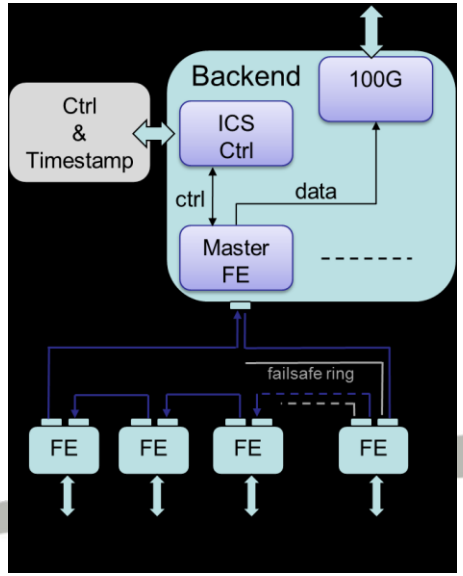


# Summary

- A Data Acquisition ring prototype has been developed.

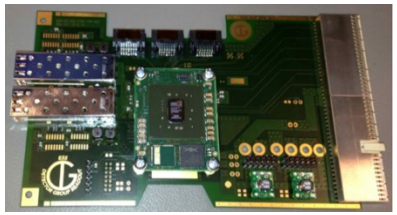


- Demonstrates 3 functions:
  - Bulk Data collection
  - Timestamp distribution ($\Delta t \sim 10ns$)
  - Memory-mapped Slow Control ("register peek/poke")

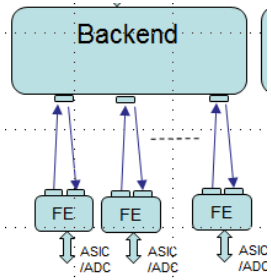



- Integrates with existing BE system
  =>

# Next Steps



- Port firmware to custom FEA hardware =>
- Simplify ring bring-up; Analyse failure modes; Improve Diagnostics; Test with more FE's on ring.
- Implement point-to-point topology. =>




- Test with ESS Timing Receiver hardware => and further develop ICS Control interface