



Science & Technology  
Facilities Council

# Update on Readout Electronics: An End-to-End Demonstrator

Dr. Harry Walton

Rutherford Appleton Laboratory, UK



EUROPEAN  
SPALLATION  
SOURCE

# Data Acquisition Electronics - I.K.C.

Collaborative partnership between

Detector Group  
Richard Hall-  
Wilton



Daresbury



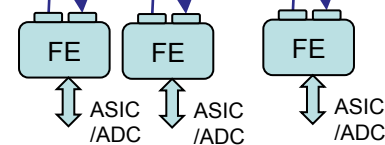
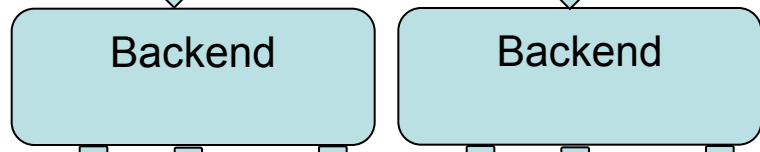
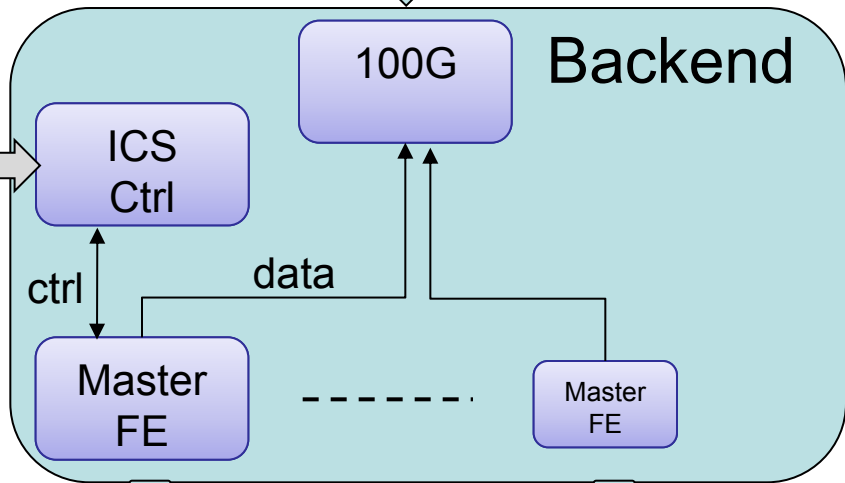
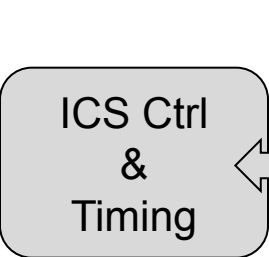
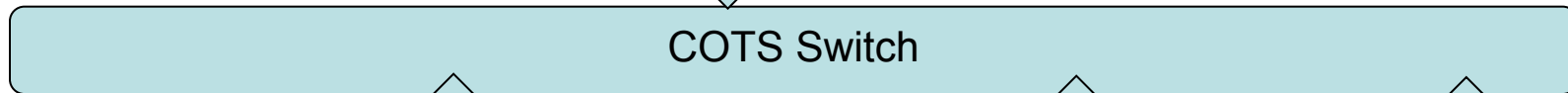
RAL,  
Technology Group,  
Marcus French



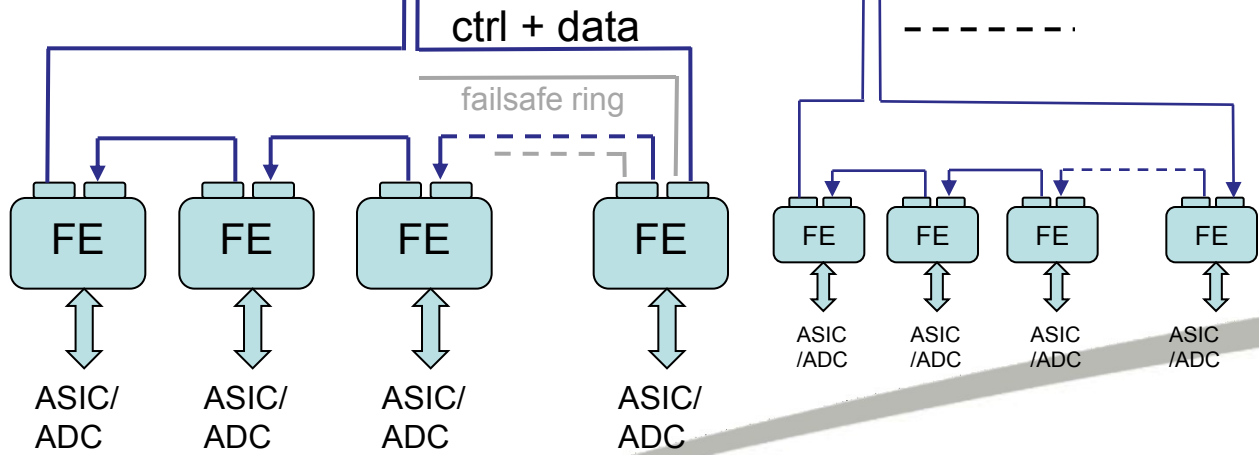


# System Architecture

↕ To DMSC



P-to-P Topology

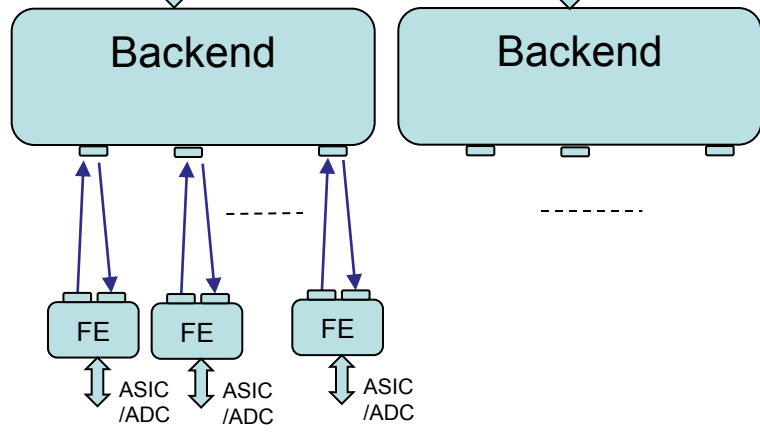
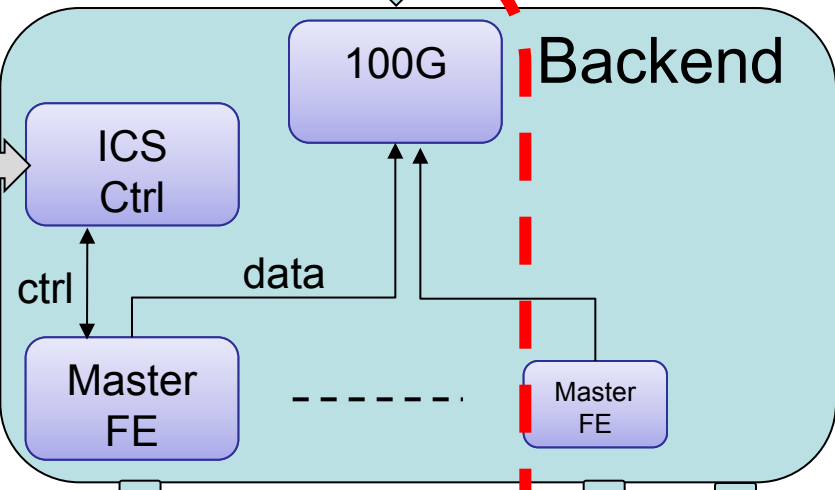


Ring Topology

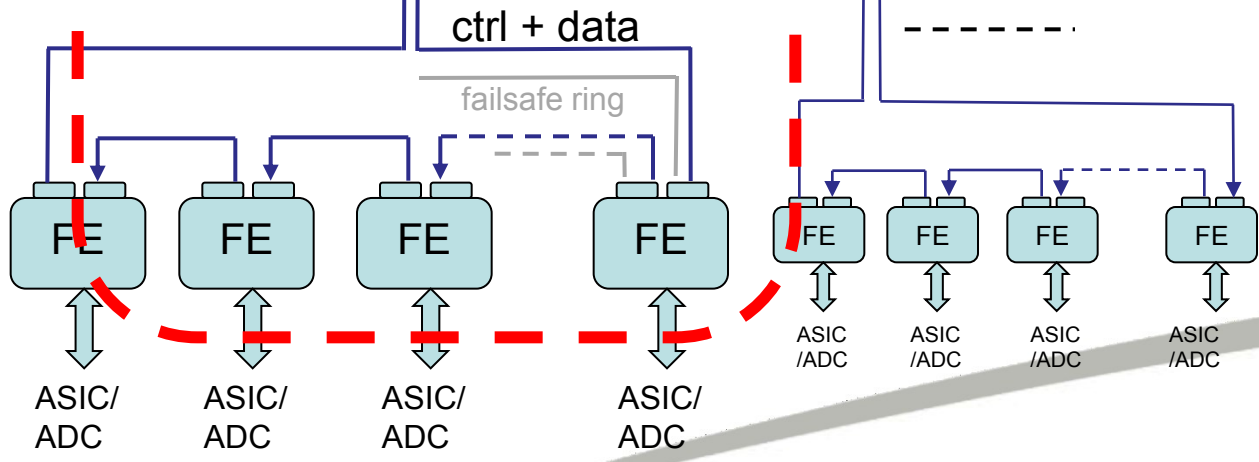
Detector Readout for ESS Instruments  
Scott Kolya, IKON-13,  
Sept.2017

# Today : An End-to-End Demonstrator

↕ To DMSC

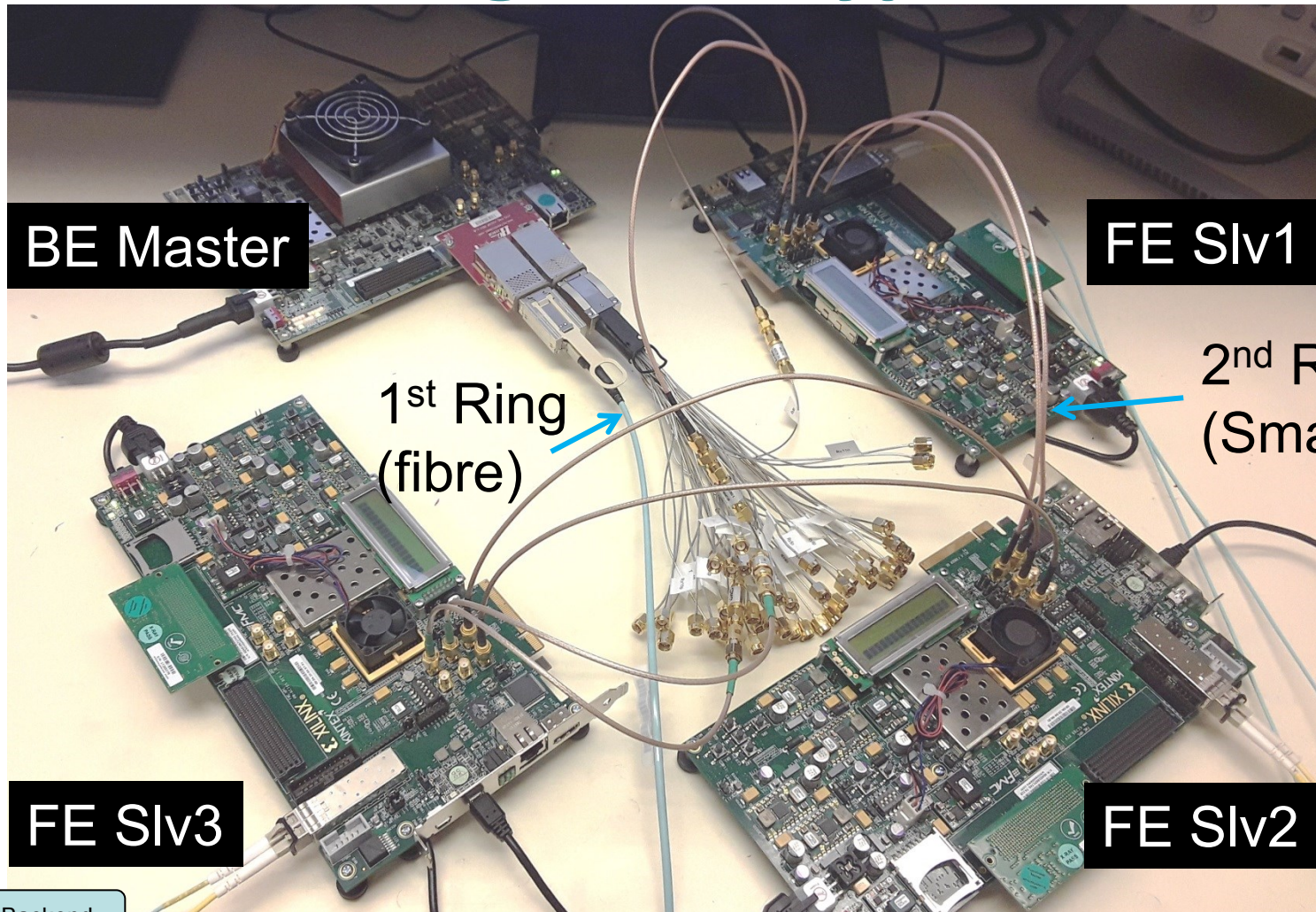


P-to-P Topology



Ring Topology

# Ring Prototype



BE Master

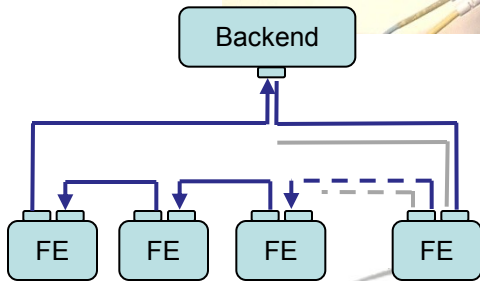
FE Slv1

1<sup>st</sup> Ring  
(fibre)

2<sup>nd</sup> Ring  
(Sma Cu)

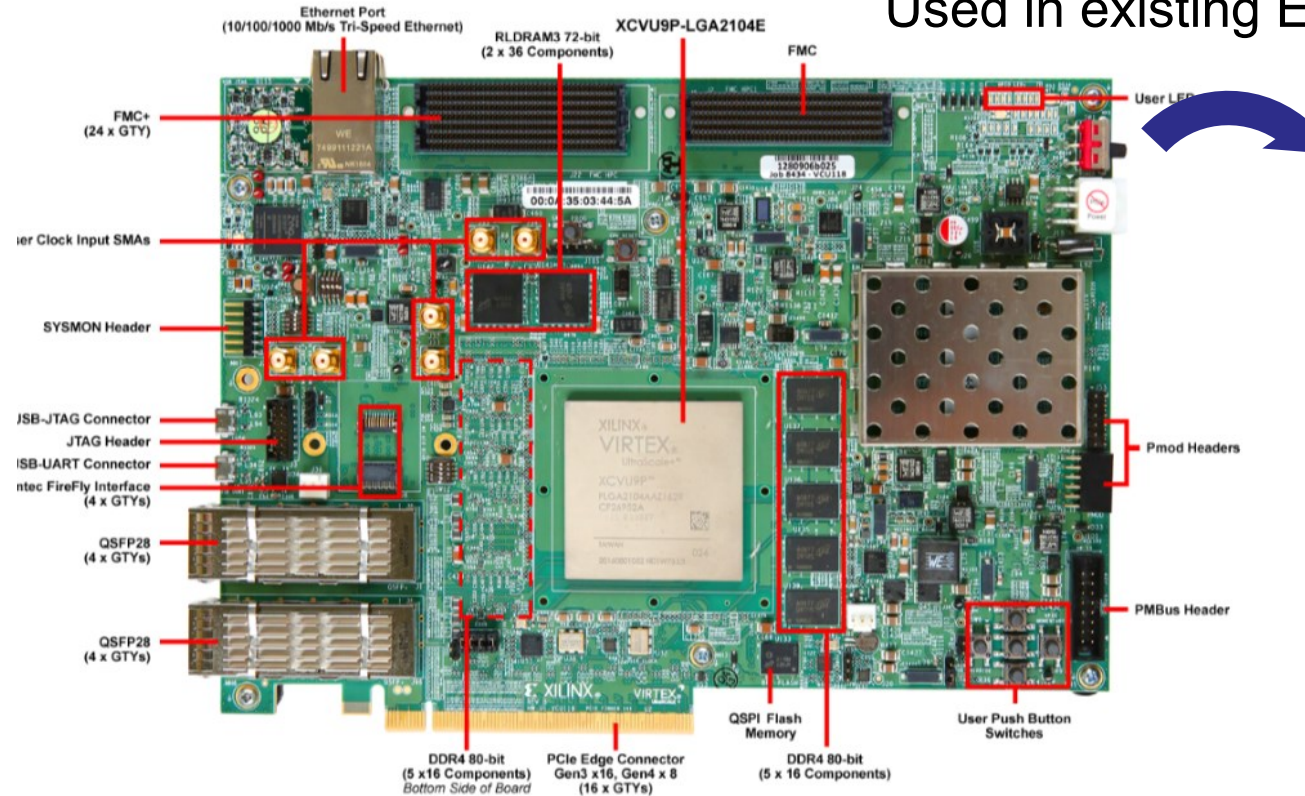
FE Slv3

FE Slv2



# Backend Hardware

Used in existing ESS BE demonstrator

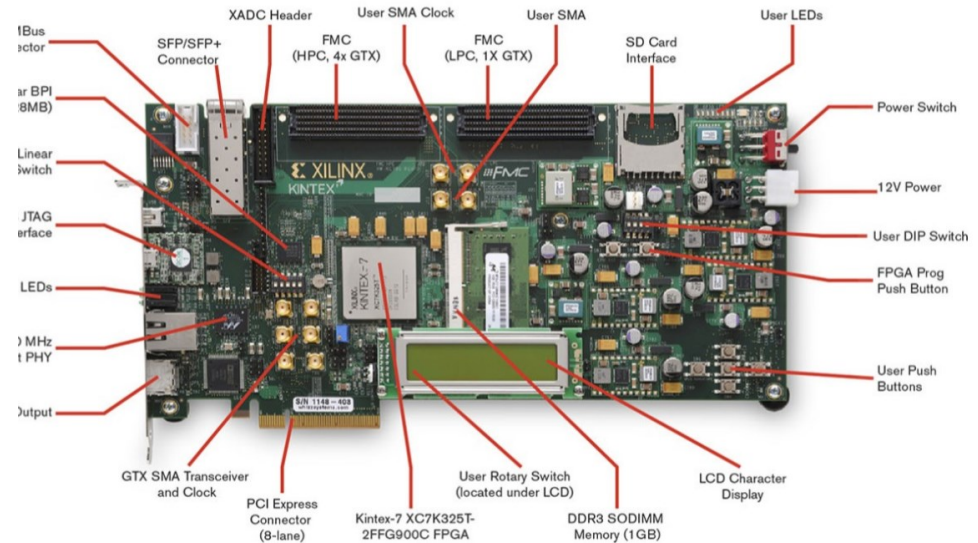


- Xilinx VCU118
- Virtex, Ultrascale+

# FE Hardware

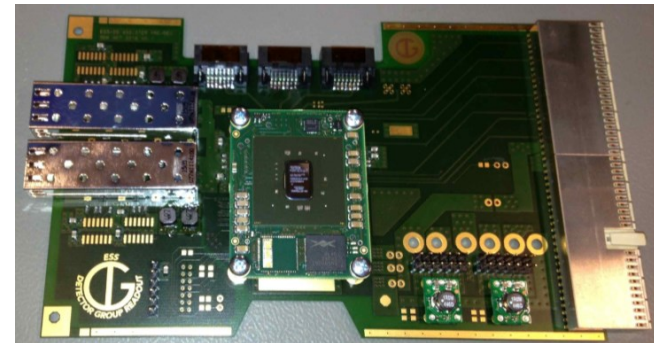
Current prototyping platform:

- Xilinx KC705
- Kintex, 7-series



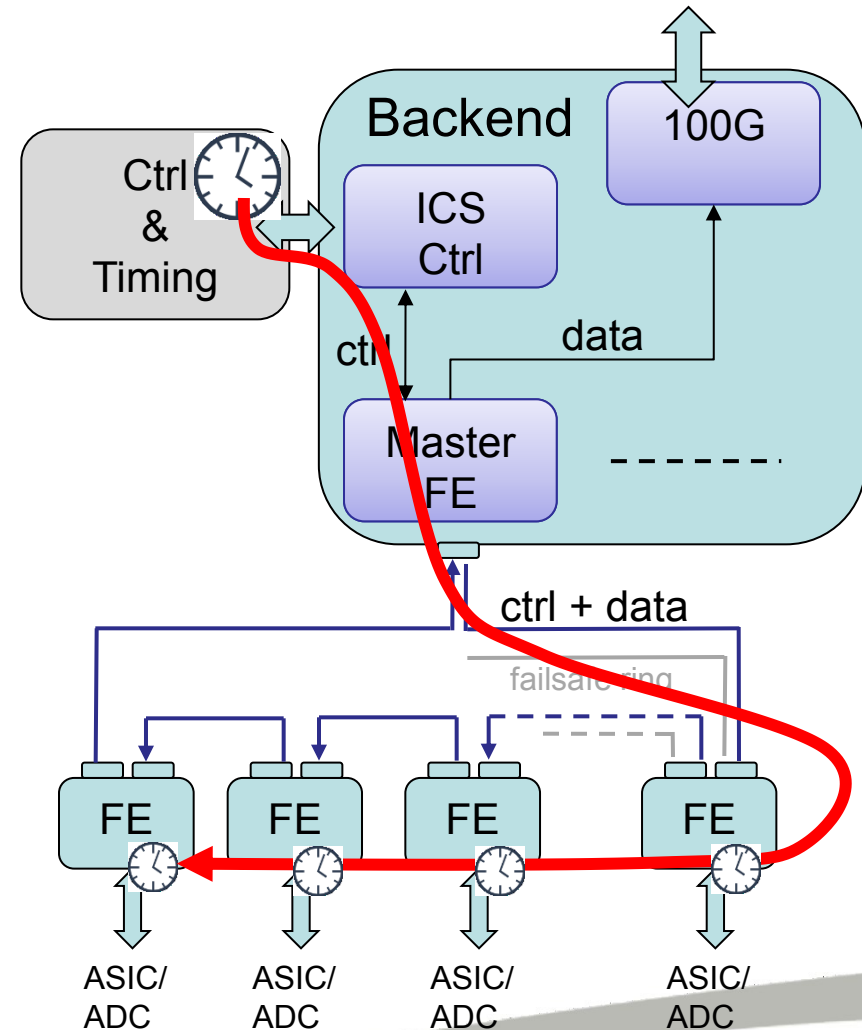
Next stage:

- Move to custom platform.



# Front End Functions

- Acquire accurate timestamp.
- Collect digitized (timestamped) neutron data, and downstream it to the BE.
- Receive & Return Slow Control data (e.g. ADC-register W/R's)

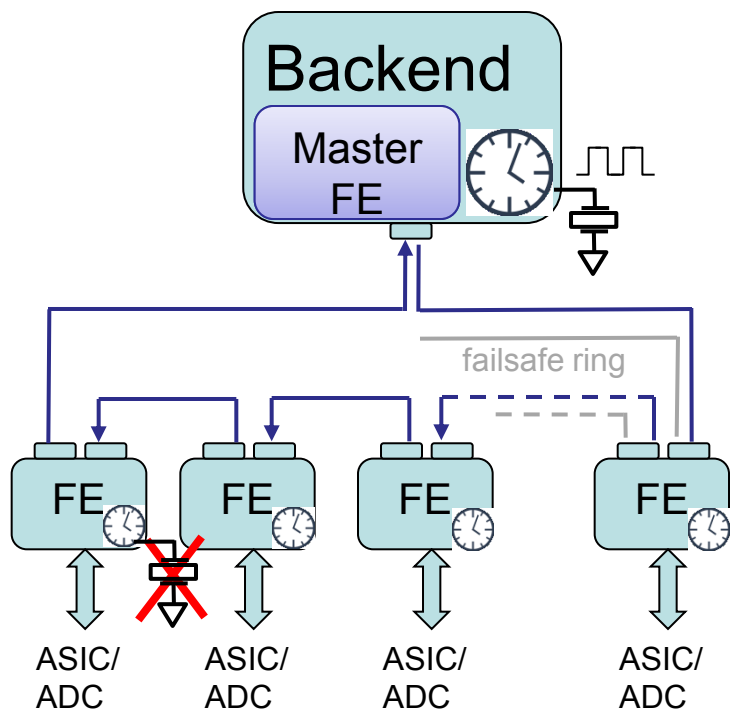




# Timestamp Challenges

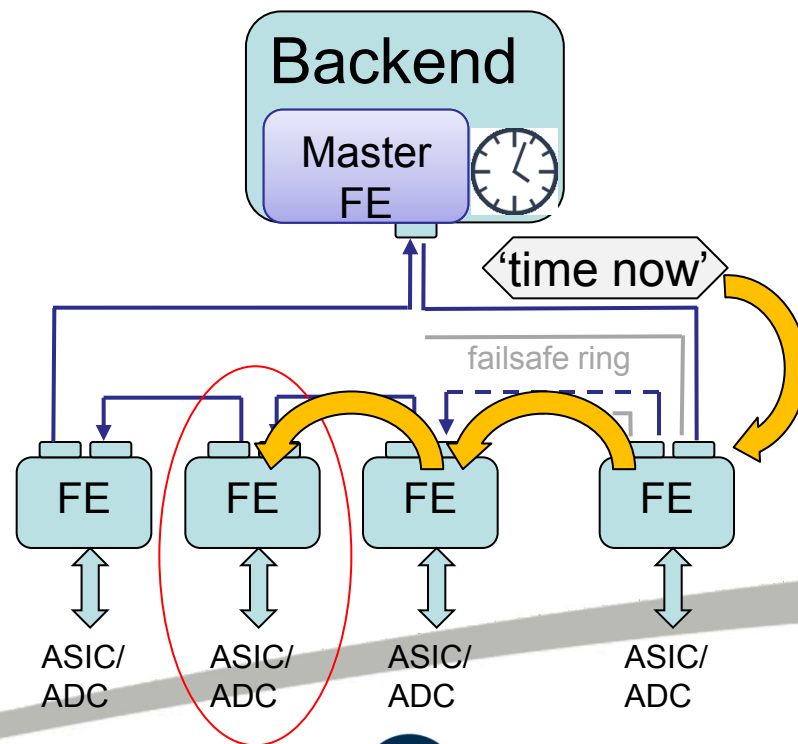
## Clock Synchronisation

Separate FPGAs must be clocked synchronously for local timestamps to 'tick' equally.



## Timestamp Distribution

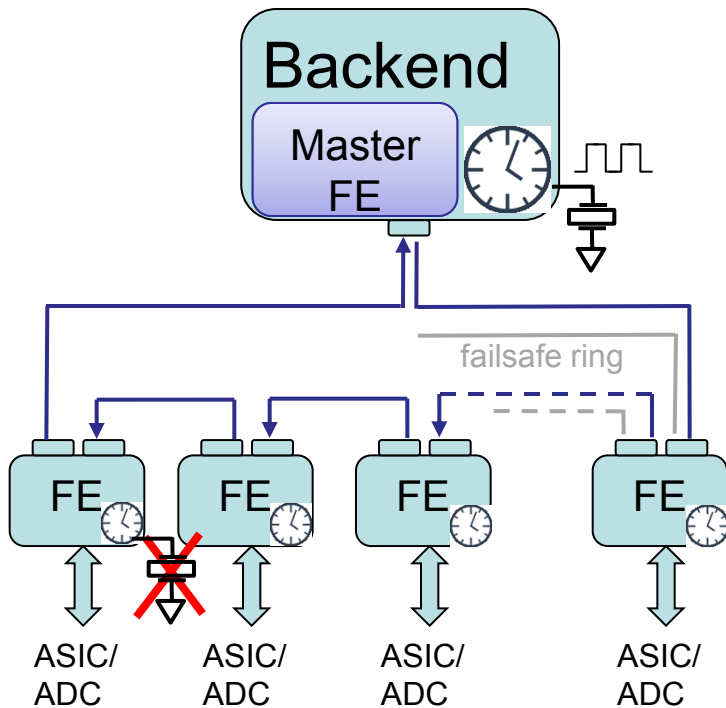
Master must allow for transit delays when initialising FE's.



# Clock Synchronisation

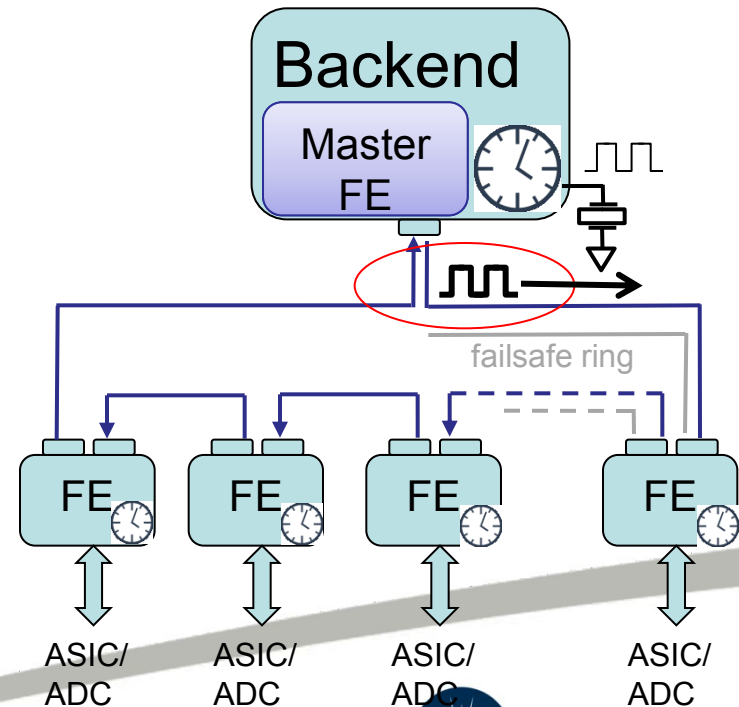
## Challenge

Local timestamps must be clocked ('tick') synchronously

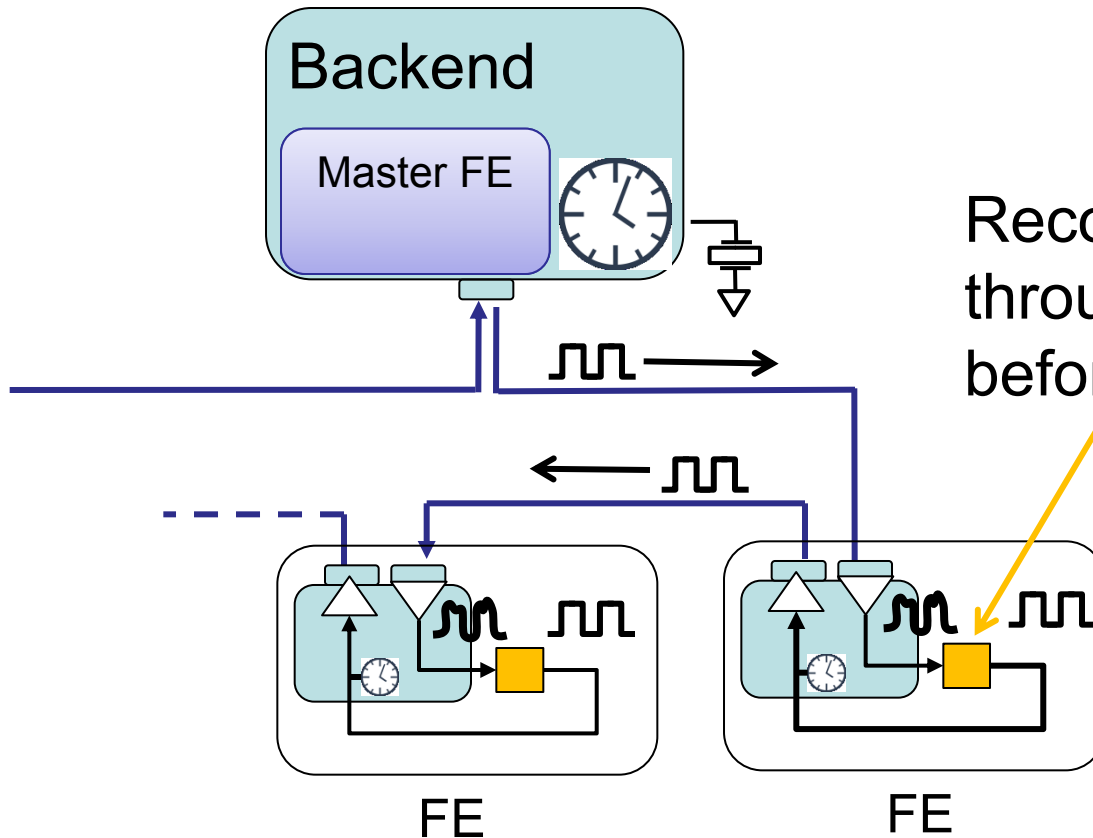


## Solution

Master embeds its clock as 8b10b bitstream. Each slave recovers and re-transmits the clock.



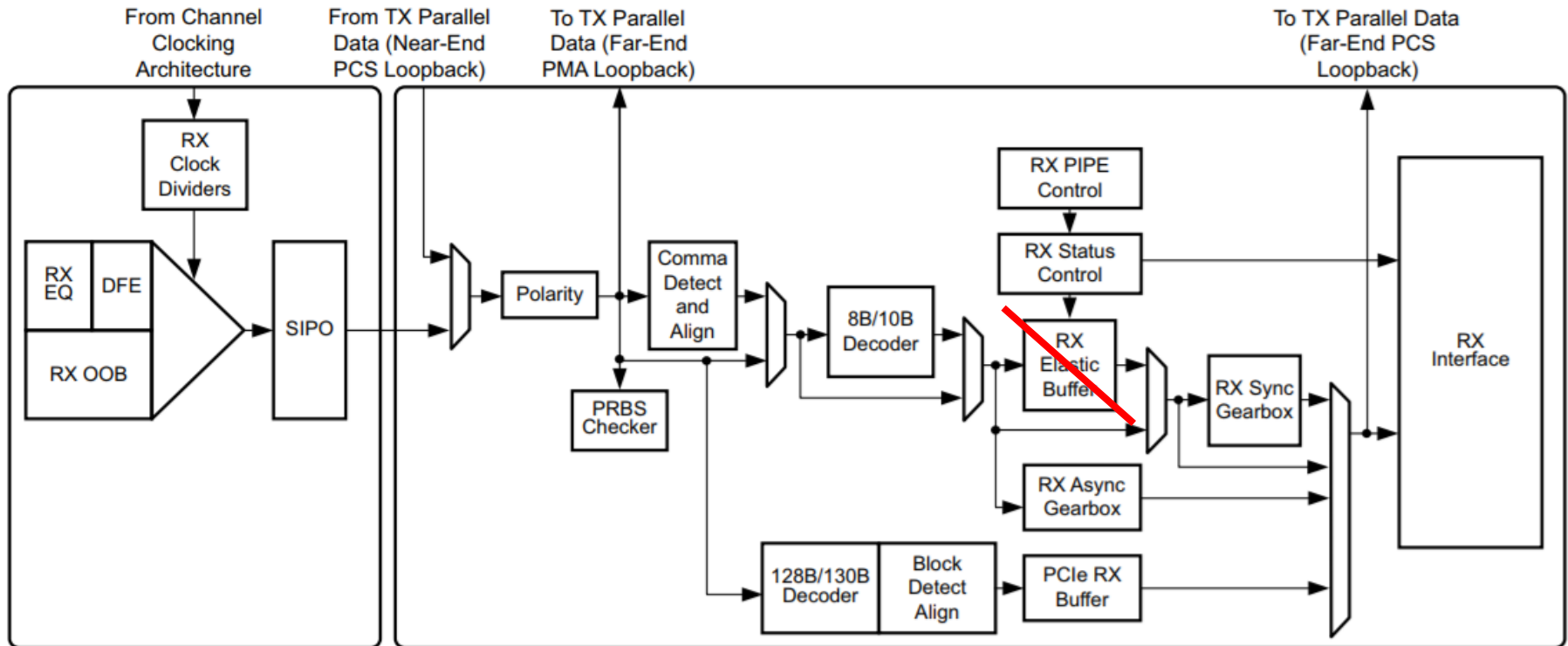
# Clock Synchronisation



Recovered clock is sent through jitter-cleaner IC before forwarding

# Clock Synchronisation

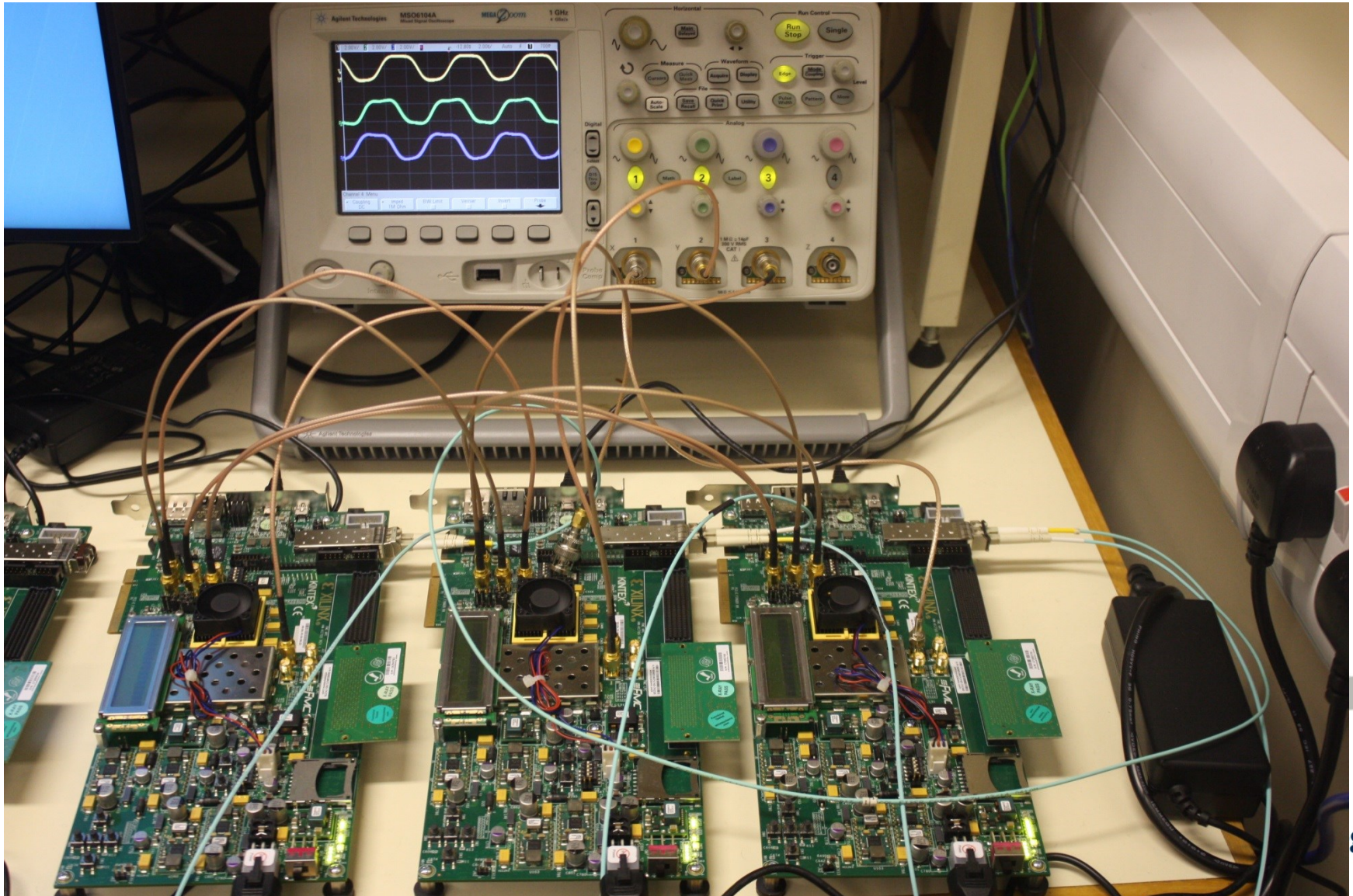
Deterministic clock recovery requires that (normally present) Elastic Buffers in FE Slave transceivers are disabled.



UG576\_c4\_01\_050217



# Clock Synchronisation - Result



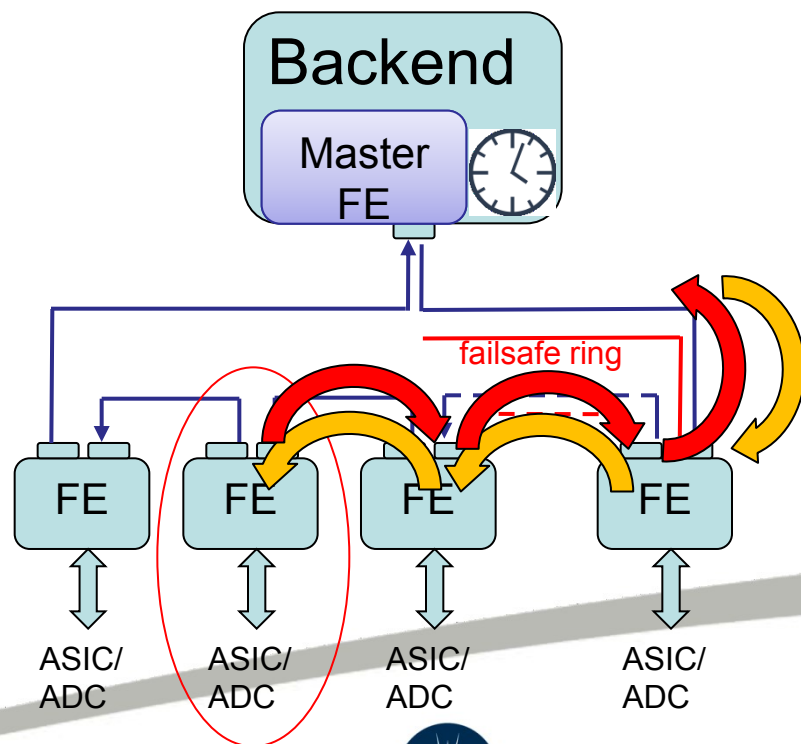
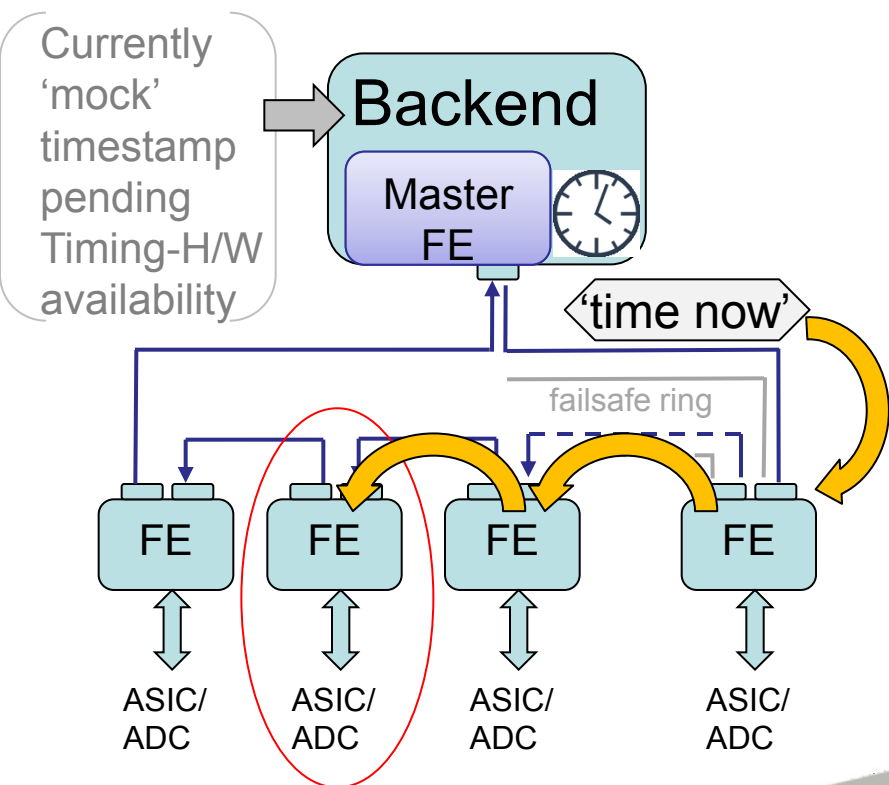
# Challenge2 – Timestamp Distribution

## Challenge

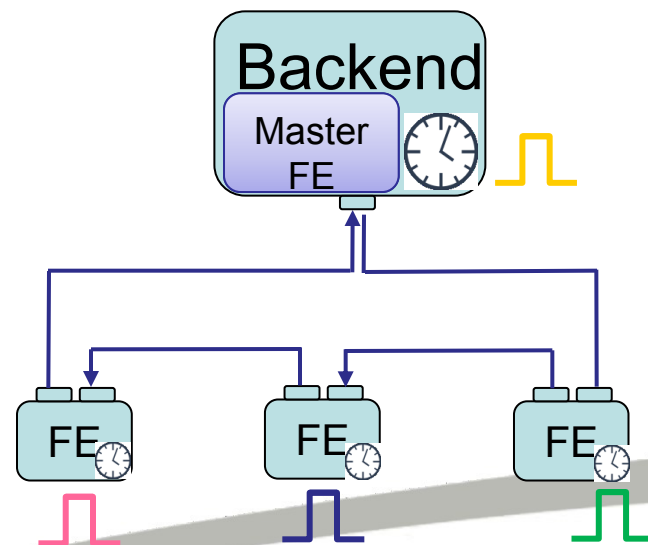
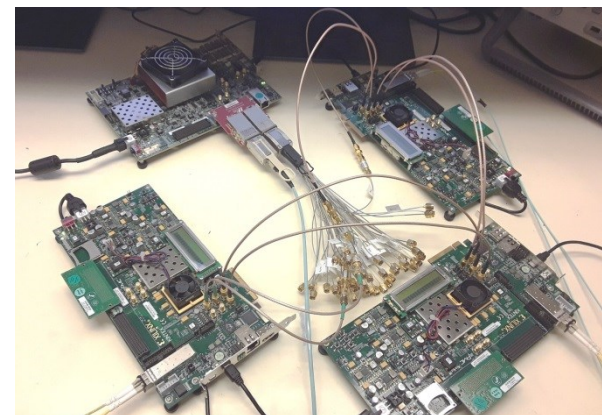
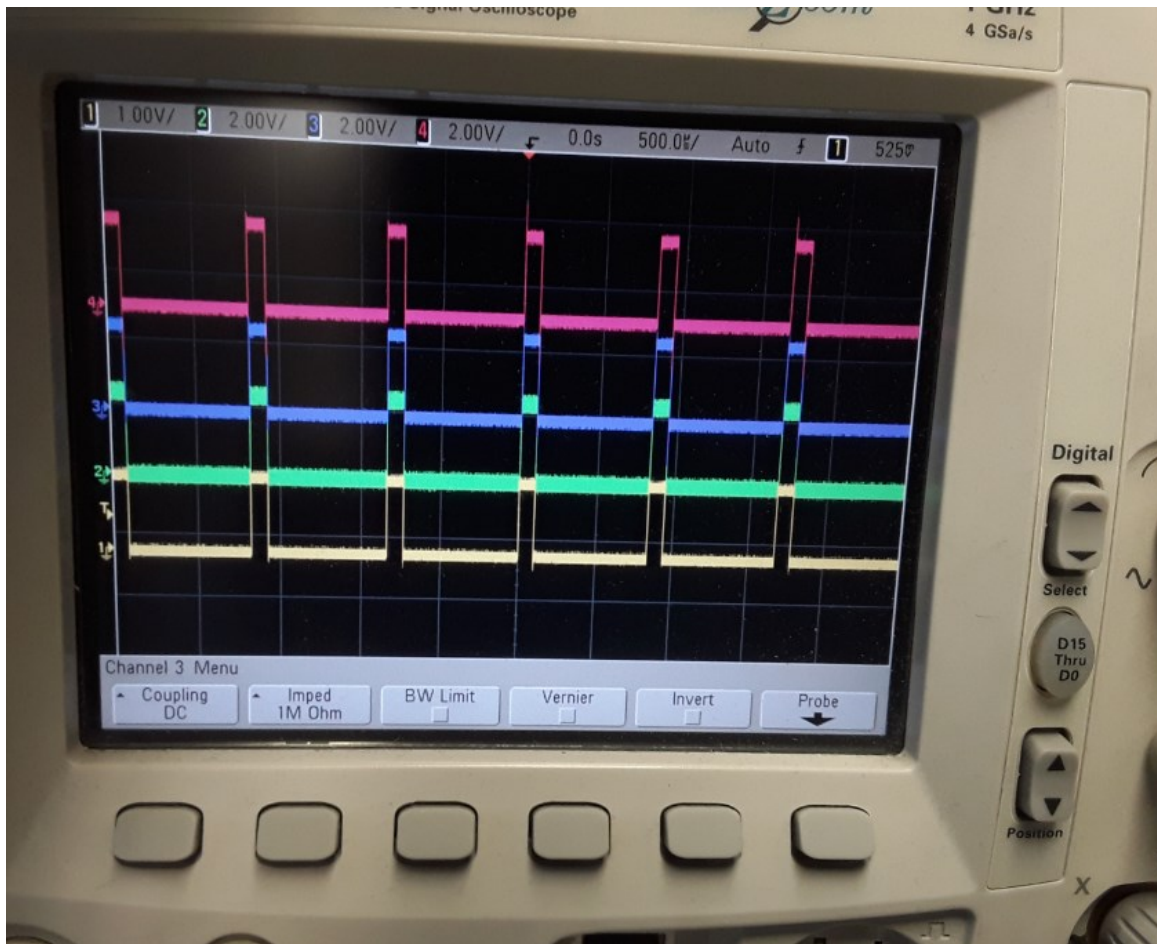
Master must allow for transit delays when initialising FE's.

## Solution

Use second ring to measure transit delays.



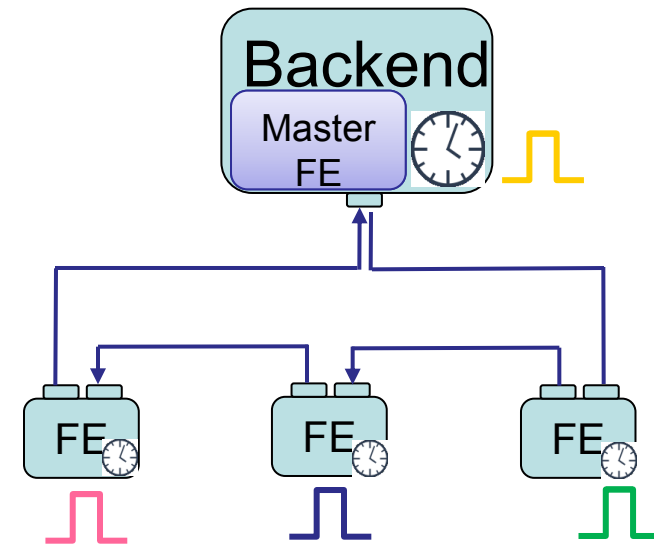
# Timestamp Synchronisation – Result



Based on local timestamp, FE's emit a pulse-per-millisecond

# Timestamp Synchronisation (detail)

Stable,  $\Delta t \sim 10\text{ns}$ , timestamp synchronisation\*



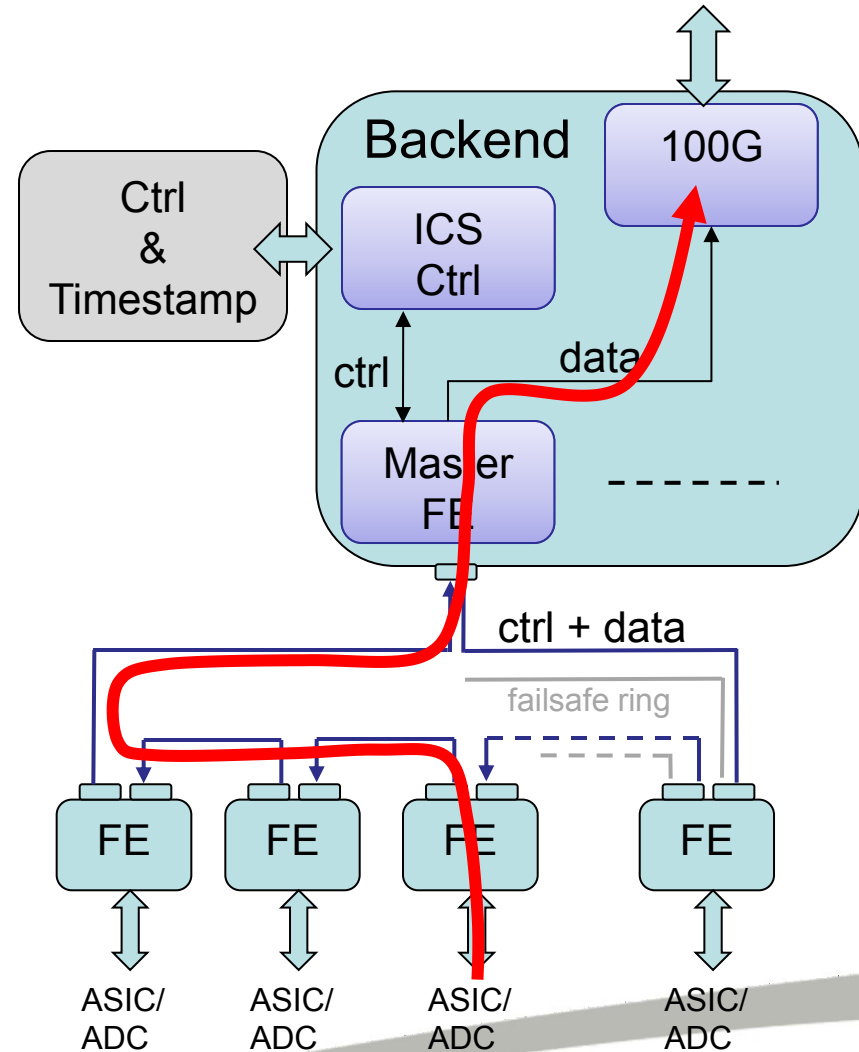
(\* c.f.  $\Delta t = 11.357\text{ns}$  requirement,

Gahl et al. *Hardware Aspects, Modularity and Integration of an Event Mode Data Acquisition and Instrument Control for the European Spallation Source (ESS)*, 2014, arXiv: 1507.01838v1)

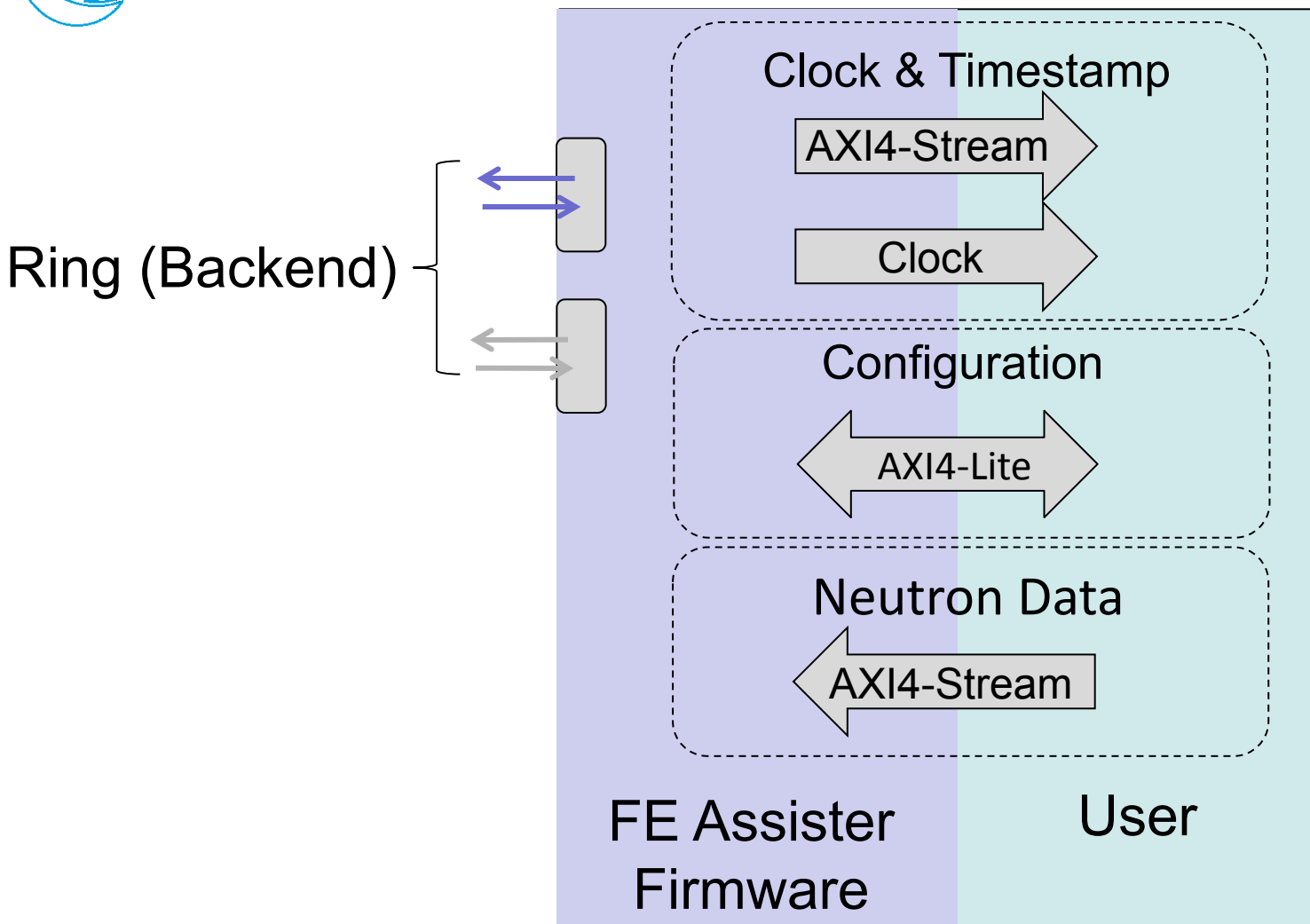


# Front End Functions

- Acquire accurate timestamp. ✓
- Collect digitized (timestamped) neutron data, and downstream it to the BE.
- Receive & Return Slow Control data (e.g. ADC-register W/R's)



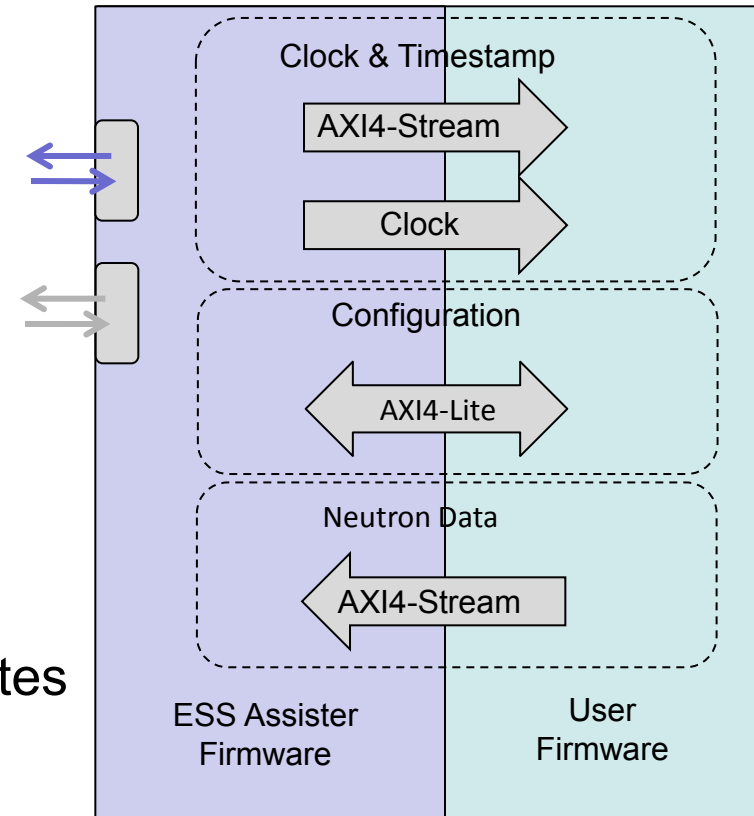
# Front End User Interface



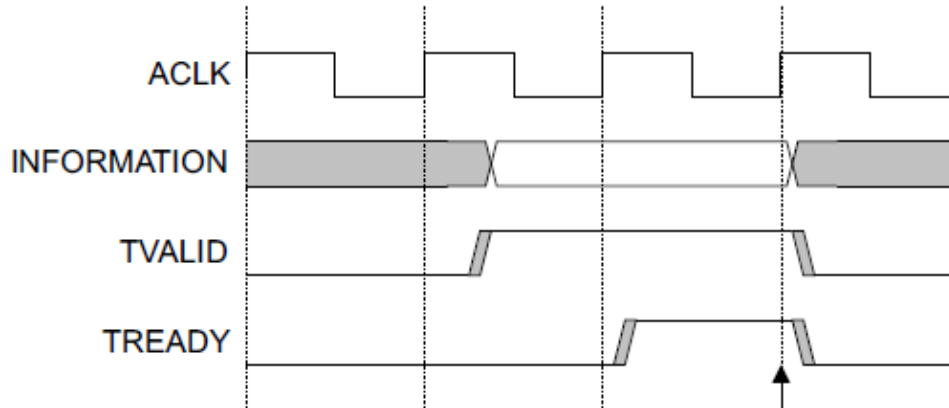
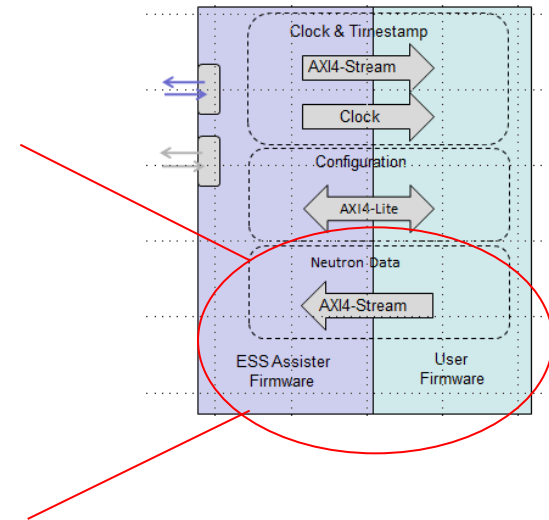
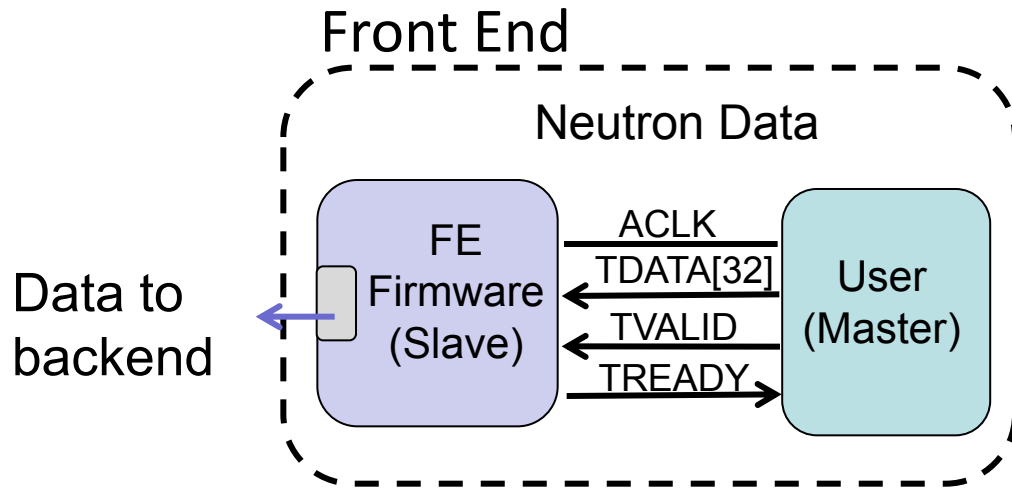
For FE integration models see  
BrightnESS Deliverable Report: D4.1 – *Integration Plan  
for Detector Readout*, Scott Kolya et.al. 2017

# AXI Interface To Users

- Originated by Arm Ltd.
- Free documentation
- Extensive support from FPGA-vendors (Xilinx).
- Various 'flavours'
  - AXI4-Stream - Simple Data Exchange
  - AXI4-Lite - Address based Read/Writes
  - AXI4 - 'Heavyweight' e.g. burst transfers etc.

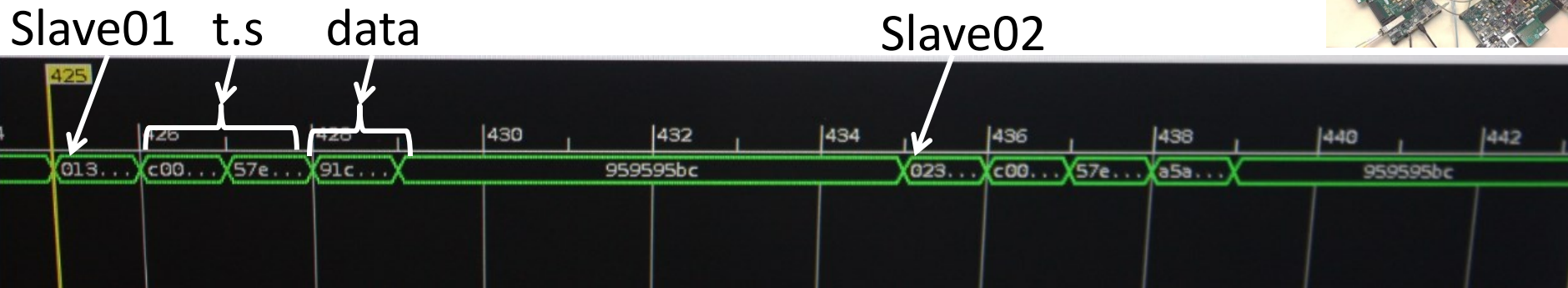
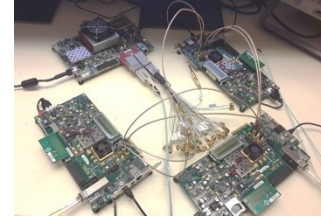


# Neutron Data AXI4-Stream I/f

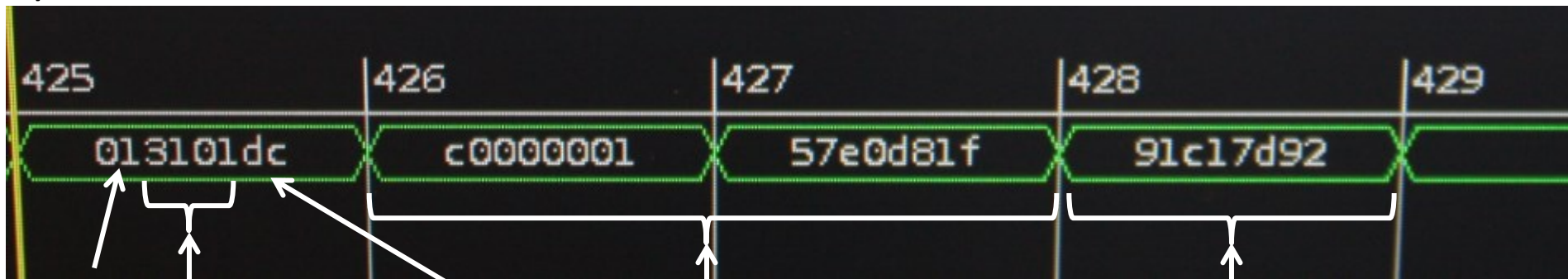


# Collecting Data - Result

A) Screenshots of data packets returning to FE Master.



B) Detail:



Slave i.d.	slave status incl. fifo level	packet type (data / control)	64-bit timestamp	32-bit Data
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# 100G Data Packets

enp2s0 [Wireshark 1.10.14 (Git Rev Unknown from unknown)]

File Edit View Go Capture Analyze Statistics Telephony Tools Internals Help

Filter: Expression... Clear Apply Save

No.	Time	Source	Destination	Protocol	Length	Info
605716	18.87824680	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605717	18.87830519	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605718	18.87830938	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605719	18.87836700	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605720	18.87837091	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605721	18.87842895	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605722	18.87843293	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605723	18.87849139	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605724	18.87849551	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605725	18.87856165	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605726	18.87856570	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605727	18.87861508	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605728	18.87862108	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605729	18.87867514	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605730	18.87868115	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605731	18.87873988	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605732	18.87874540	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605733	18.87880176	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650
605734	18.87880679	192.168.9.15	192.168.9.1	UDP	9204	Source port: 61649 Destination port: 61650

```

0000 e4 1d 2d ab c5 28 00 0a 35 03 5b 91 08 00 45 00  ....(.. 5.[...E.
0010 23 e6 00 00 00 00 05 11 fe a6 c0 a8 09 0f c0 a8  #.....#.....#...
0020 09 01 f0 d1 f0 d2 23 d2 00 00 fe ed 23 ca 92 82  .....#.....#...
0030 fa ce ee ee 00 00 00 00 00 00 00 01 00 00 00 02  .....#.....#...
0040 00 00 00 03 00 00 00 04 00 00 00 05 00 00 00 06  .....#.....#...
0050 00 00 00 07 00 00 00 08 00 00 00 09 00 00 00 0a  .....#.....#...
0060 00 00 00 0b 00 00 00 0c 00 00 00 00 00 00 00 01  .....#.....#...
0070 00 00 00 02 00 00 00 03 00 00 00 04 00 00 00 05  .....#.....#...
0080 00 00 00 06 00 00 00 07 00 00 00 08 00 00 00 09  .....#.....#...
0090 00 00 00 0a 00 00 00 0b 00 00 00 0c 00 00 00 00  .....#.....#...
00a0 00 00 00 01 00 00 00 02 00 00 00 03 00 00 00 04  .....#.....#...
00b0 00 00 00 05 00 00 00 06 00 00 00 07 00 00 00 08  .....#.....#...
00c0 00 00 00 09 00 00 00 0a 00 00 00 0b 00 00 00 0c  .....#.....#...
00d0 00 00 00 00 00 00 00 01 00 00 00 02 00 00 00 03  .....#.....#...
00e0 00 00 00 04 00 00 00 05 00 00 00 06 00 00 00 07  .....#.....#...
00f0 00 00 00 08 00 00 00 09 00 00 00 0a 00 00 00 0b  .....#.....#...
0100 00 00 00 0c 00 00 00 00 00 00 00 01 00 00 00 02  .....#.....#...
0110 00 00 00 03 00 00 00 04 00 00 00 05 00 00 00 06  .....#.....#...

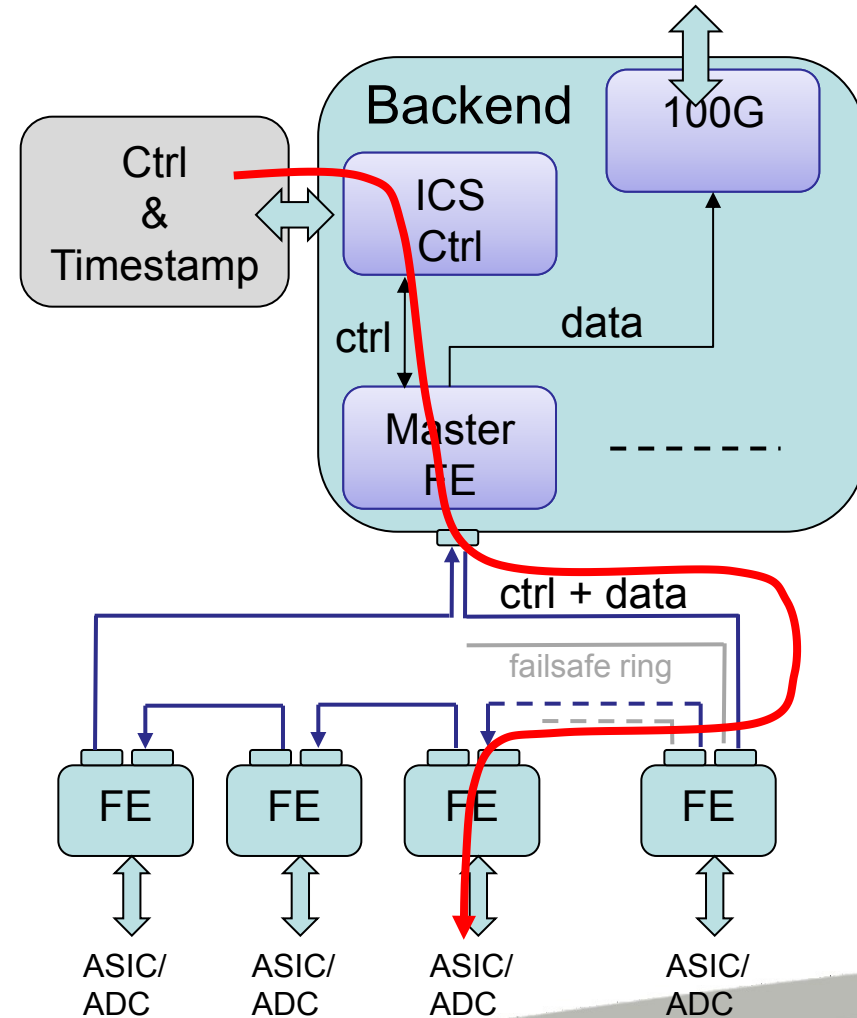
```

File: "/tmp/wireshark\_pcapng\_enp2s... Packets: 605735 · Displayed: 605735 (100.0%) · Dropped: 29 (0.0%) Profile: Default



# Front End (FE) Functions

- Acquire accurate timestamp.
- Collect digitized (timestamped) neutron data, and downstream it to the BE. ✓
- Receive & Return Control data (e.g. ADC-register W/R's)

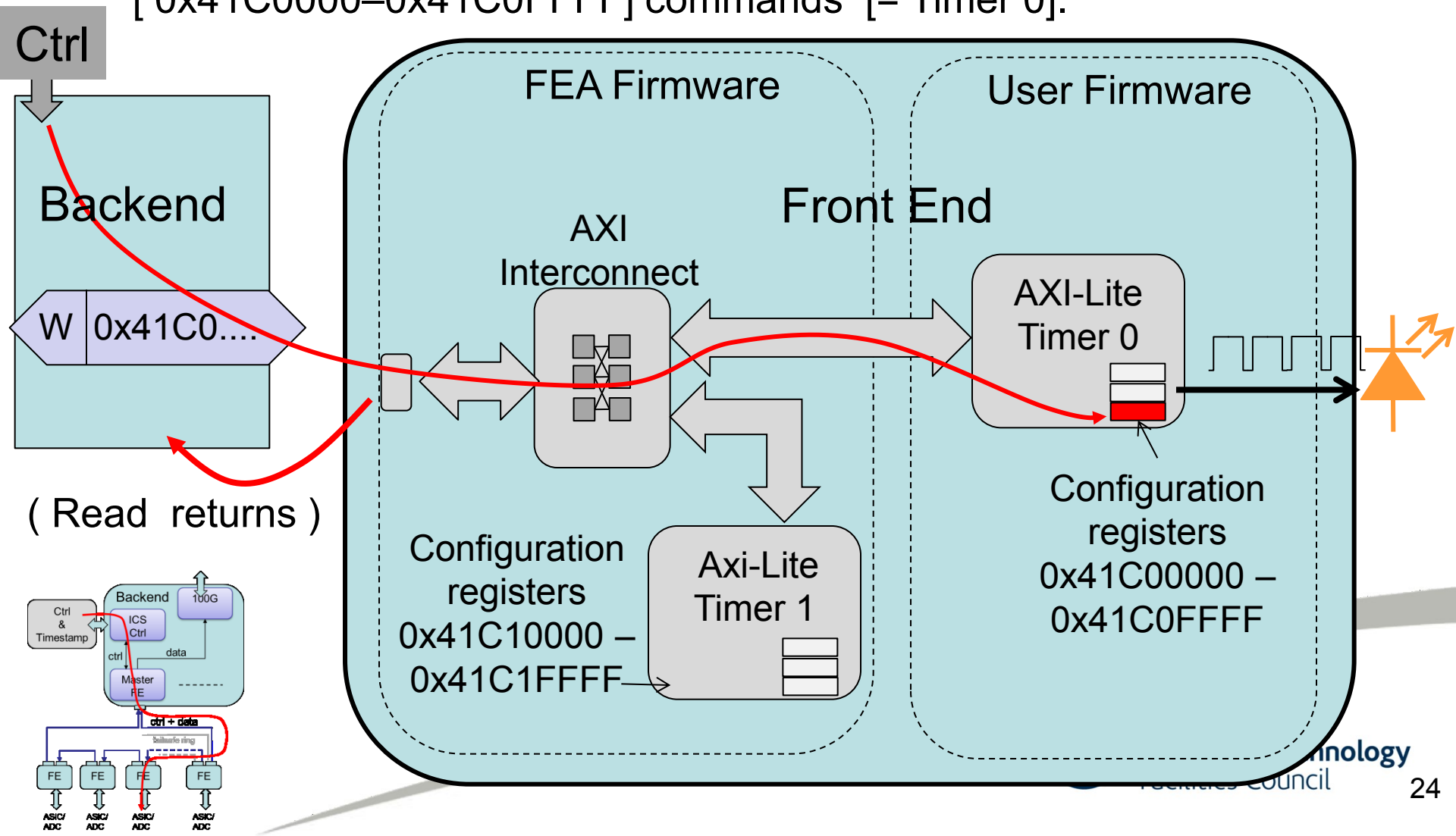




# Memory-mapped Slow Control –

## Example:

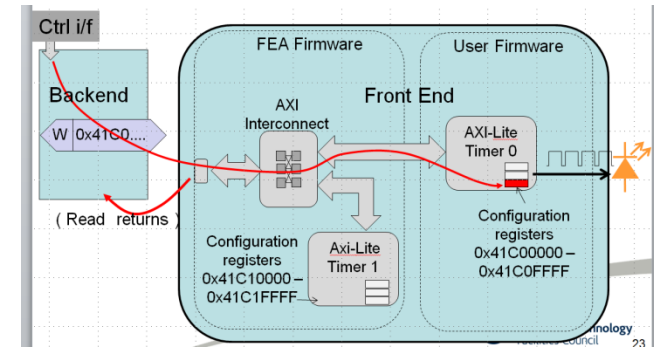
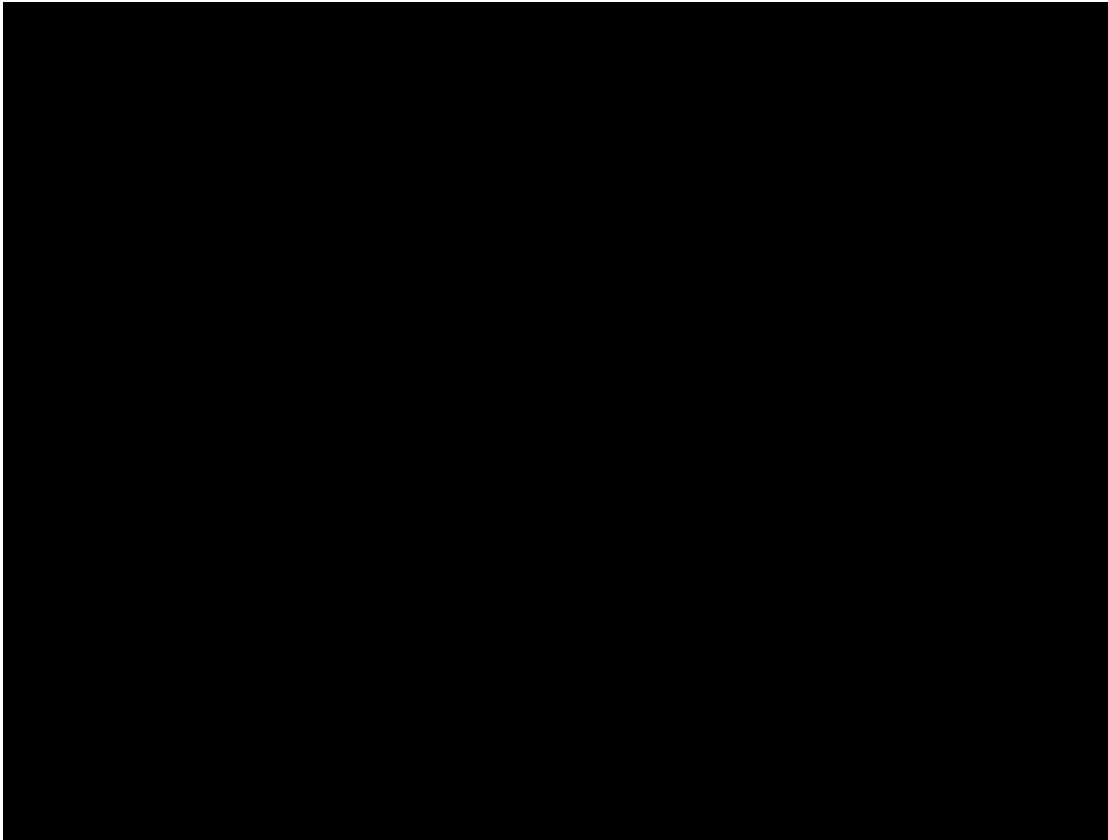
Backend launches packets onto ring containing “write-to-memory” [ 0x41C0000–0x41C0FFFF] commands [= Timer 0].



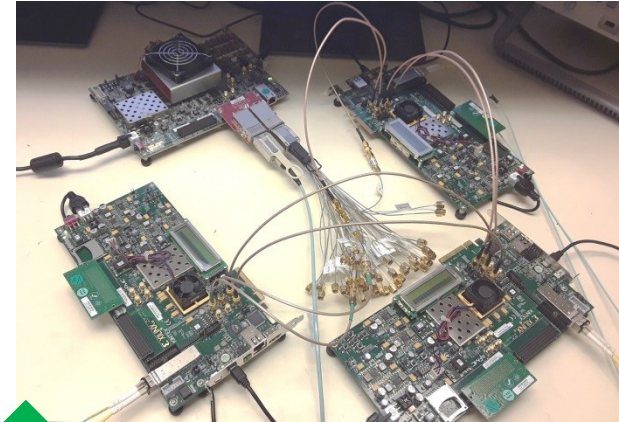




# Memory-mapped Slow Control Example

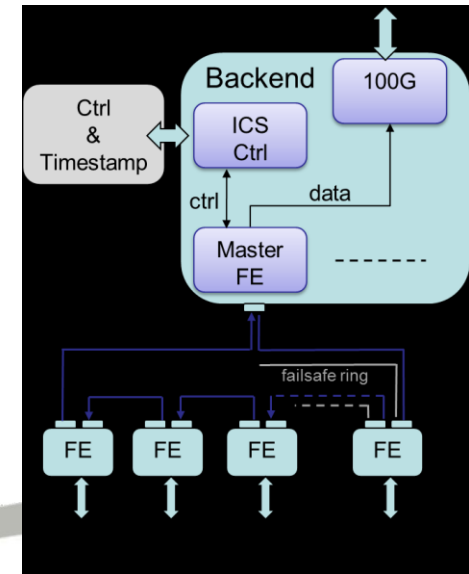


# Summary



- A Data Acquisition ring prototype has been developed.
- Demonstrates 3 functions:
  - Bulk Data collection ✓
  - Timestamp distribution ( $\Delta t \sim 10\text{ns}$ ) ✓
  - Memory-mapped Slow Control (“register peek/poke”) ✓
- Integrates with existing BE system

=>



# Next Steps

- Port firmware to custom FEA hardware =>
- Simplify ring bring-up; Analyse failure modes; Improve Diagnostics; Test with more FE's on ring.
- Implement point-to-point topology. =>
- Test with ESS Timing Receiver hardware => and further develop ICS Control interface

