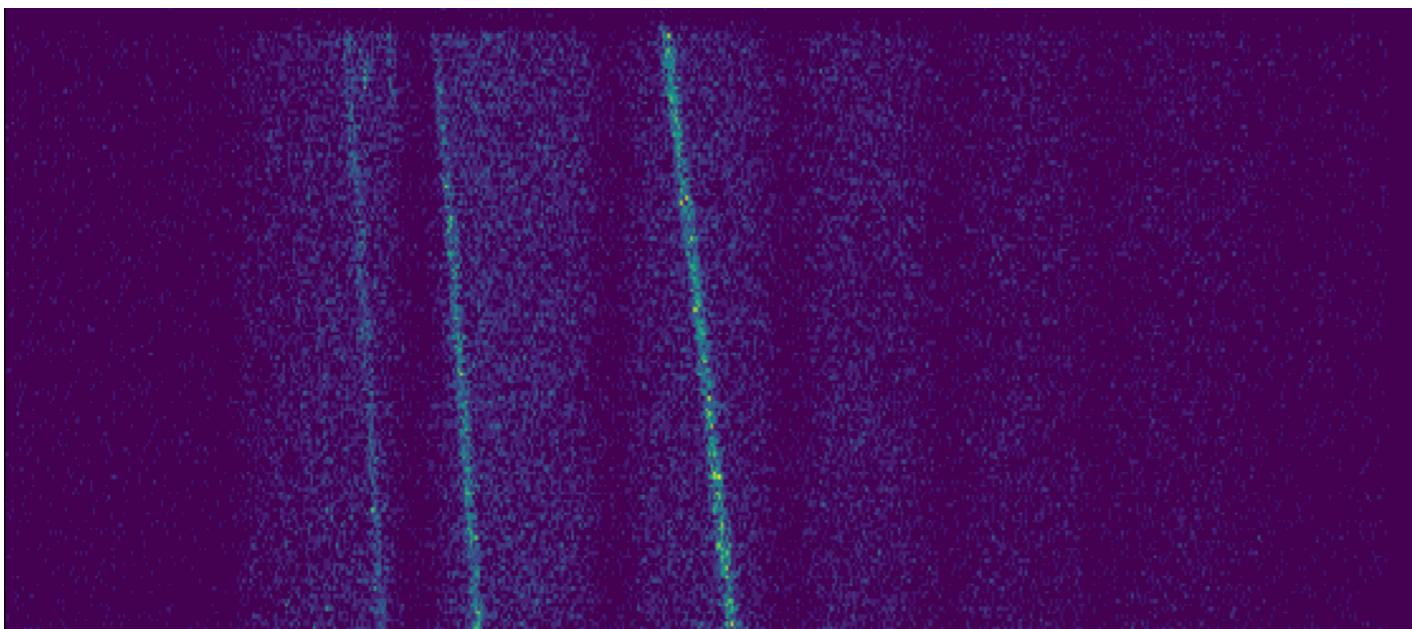
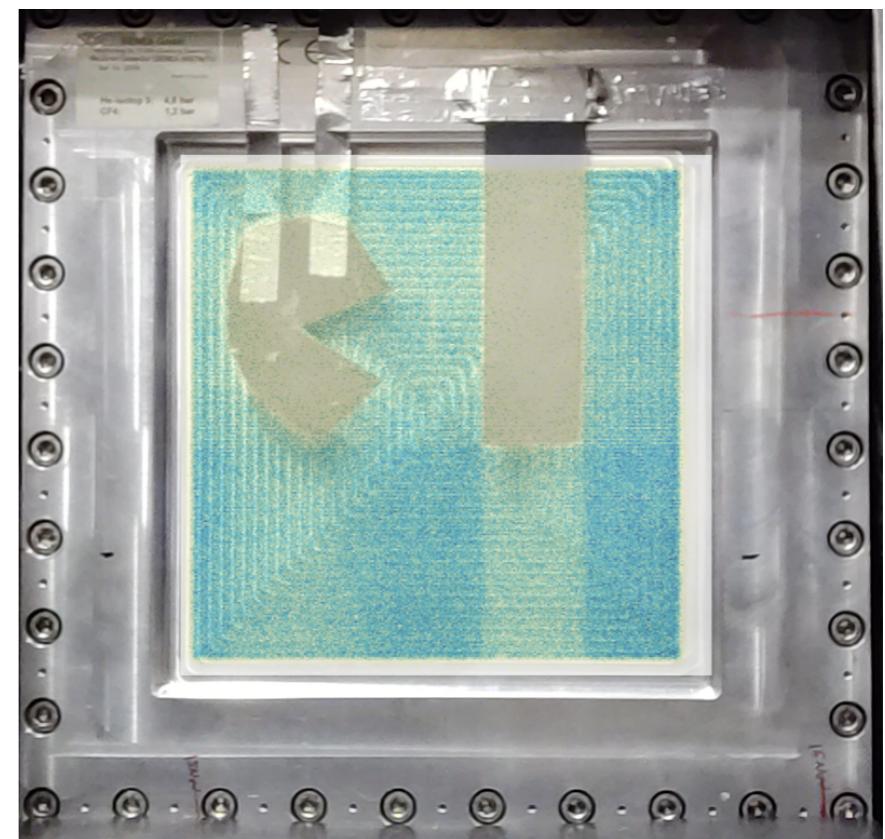
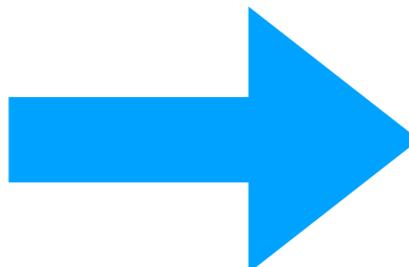
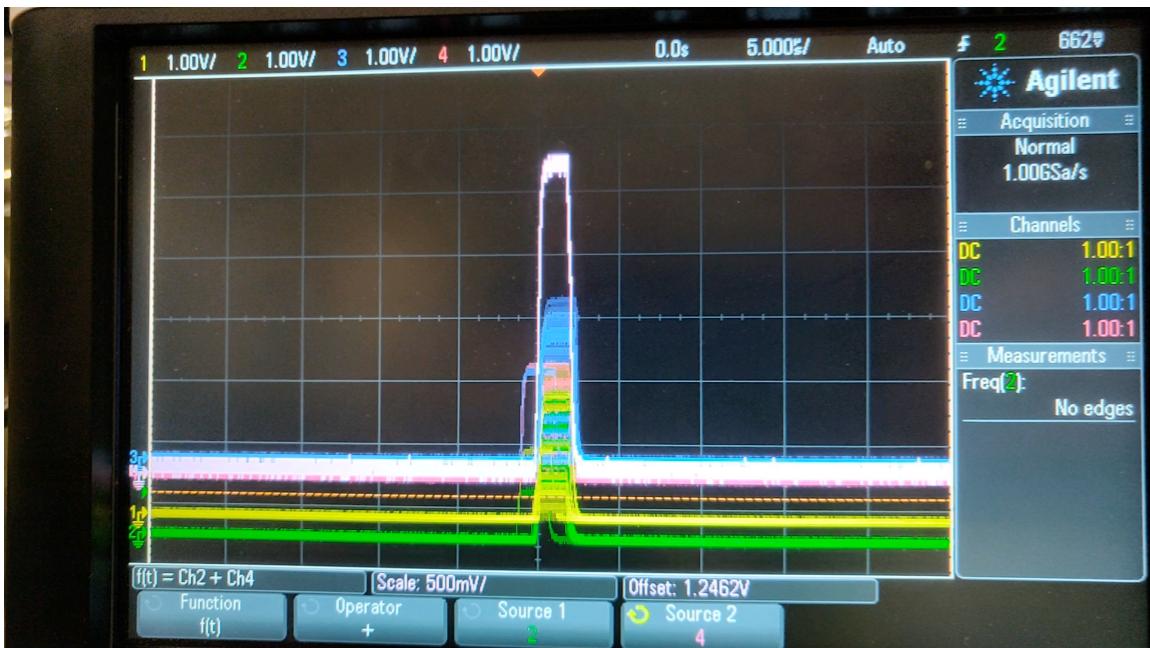


EPICS Control - Lessons from V20 and Way Forward

HZB V20 Results

Data processing pipeline from start to finish

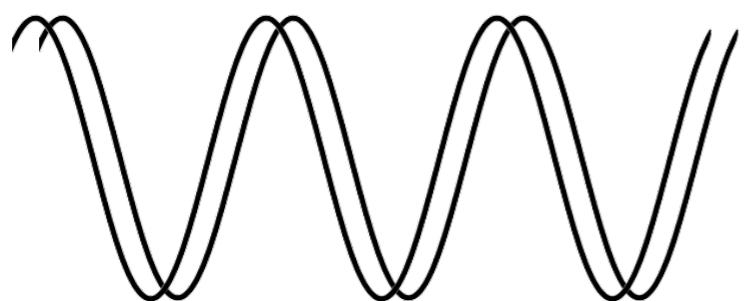


Success!

Lessons learned from V20 test



- We need a good EPICS interface for control/configuration of readout system



- We need to be able to verify that the readout hardware is synchronised to the timing system



- We need to be able to test the readout system without access to the timing system

Configuration of the FPGA

0 git_hash LW	26 udp_dst_port LW
1 build_time TIME	27 pkt_timeout LW
2 device_id_h LW	28 ch0_gain GAIN
3 device_id_m LW	29 ch1_gain GAIN
4 device_id_l LW	30 ch2_gain GAIN
5 loopback LW	31 ch3_gain GAIN
6 rst_vec LW	32 ch0_offset OFFSET
7 adc_chsel LW	33 ch1_offset OFFSET
8 adc_dec LW	34 ch2_offset OFFSET
9 adc_bypass_zs LW	35 ch3_offset OFFSET
10 adc_thresh_0 LW	36 adc_spi LW
11 adc_thresh_1 LW	37 si570_base LW
12 adc_thresh_2 LW	38 si570_data LW
13 adc_thresh_3 LW	39 si570_trig LW
14 adc_rhold_b2 LW	40 led_sel LW
15 adc_fhold_b2 LW	41 pulse_cnt_01 LW
16 adc_sampsb_b2 LW	42 pulse_cnt_23 LW
17 adc_samps_a_b2 LW	43 frm_cnt_01 LW
18 adc_mingap_b2 LW	44 frm_cnt_23 LW
19 eth_src_mac MAC	45 pkt_cnt LW
21 eth_dst_mac MAC	46 ch01_snap LW
23 ip_src_addr IP	47 ch23_snap LW
24 ip_dst_addr IP	48 status_0 LW
25 udp_src_port LW	49 status_1 LW
	50 status_2 LW

- ~50 registers
- ~50 functionalities
- Recent improvements to EPICS interface

Configuration of the FPGA

ADC Demonstrator (HZB-V20:TS-RO1:)

Basic controls

Sampling mode: Peak detect (selected), Continuous

Clock source: Internal, External

Payload source: Synthetic, ADC

Enable, Disable

Network settings

Keep alive: <ca://HZB>, <ca://HZB>

Source: <ca://HZB-V>, <ca://HZB>

Destination: <ca://HZB-V>, <ca://HZB>

IP Address: <ca://HZB-V>, <ca://HZB>

UDP Port: <ca://HZB-V>, <ca://HZB>

MAC Address: <ca://HZB-V>, <ca://HZB>

Stats and information

Table:

Name	Value
Click to add row	

< >

ADC Channels settings and stats

#	Active	Gain	Offset	Threshold	Pulses	Frames
1	<input checked="" type="checkbox"/>	No	<ca://HZ>	<ca://H>	<ca://HZ>	<ca://H>
2	<input checked="" type="checkbox"/>	No	<ca://HZ>	<ca://H>	<ca://HZ>	<ca://H>
3	<input checked="" type="checkbox"/>	No	<ca://HZ>	<ca://H>	<ca://HZ>	<ca://H>
4	<input checked="" type="checkbox"/>	No	<ca://HZ>	<ca://H>	<ca://HZ>	<ca://H>

Time synchronisation

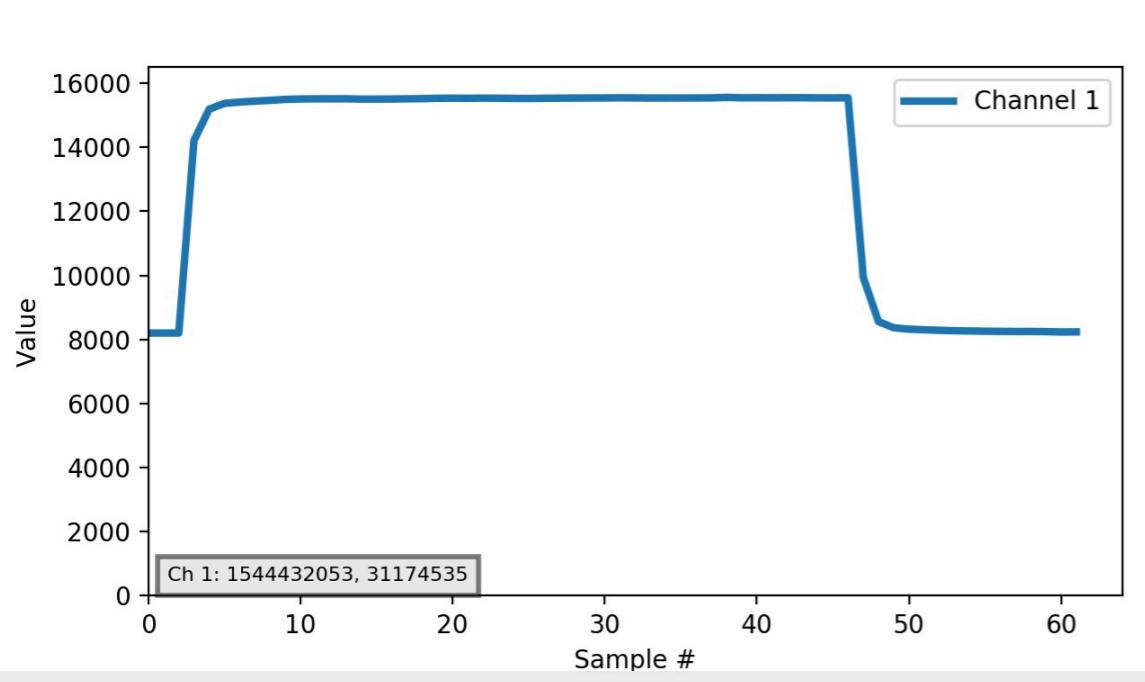
Test at HZB

Event time:

2018-12-10

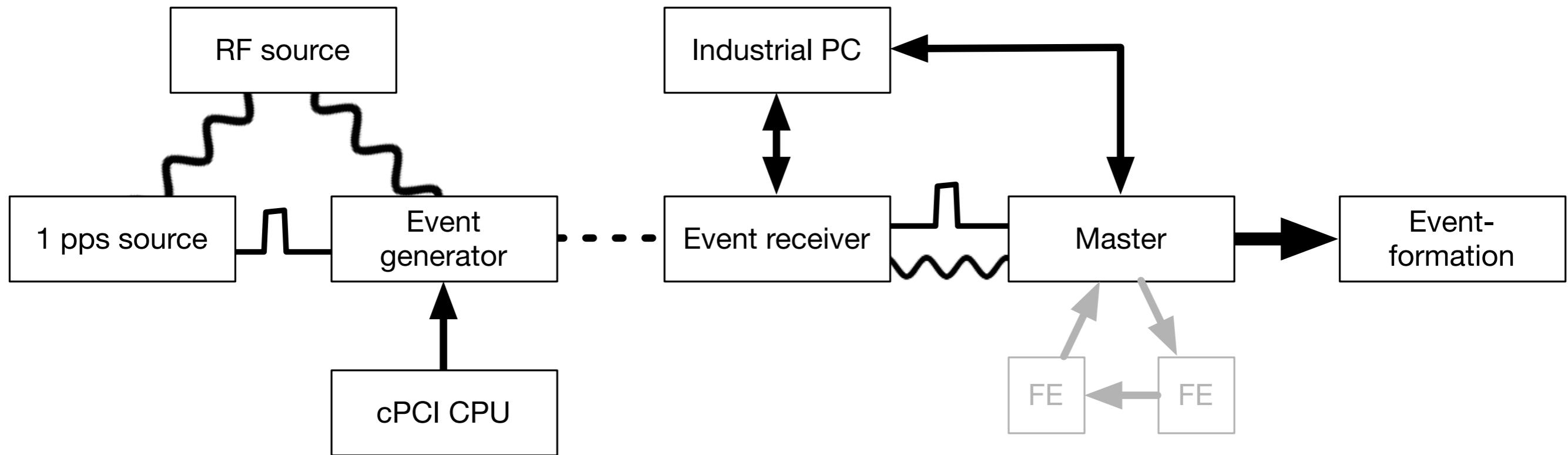
08:54:13.708082916

1. Pulse analog input of ADC using EVR
 2. Determine timestamp of pulse at EVR
 3. Determine timestamp of pulse at ADC
 4. Compare timestamps
- Result: The ADC **might** have been $\sim 7 \mu\text{s}$ out of sync with the timing system



Time synchronisation

Possible failure locations



Requirements for future tests

- Use internal oscillator without updating the firmware
- Update time counter without access to timing hardware
- We need to be able to test the readout system without access to the timing system
- Minimal to no set-up should be required to get the system up and running