Low latency link development and MPS interface

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on behalf of:

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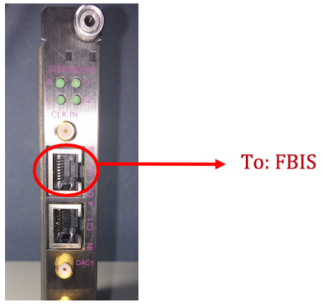
Background

BCM system has 3 special interfaces to external systems:

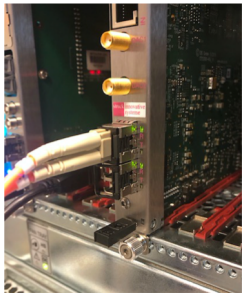
- BCM-FBIS interface:

  LVDS port on the SIS8300-KU



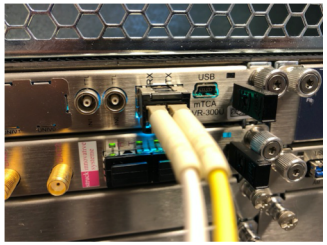
- Optical interface for sending BCM data to other crates:

  SFP port on the SIS8300-KU



- Timing:

  From EVR over the crate backplane



BCM – FBIS interface

The BCM system sends the following signals to the FBIS:

- Beam Permit (redundant): OK / NOK
- BCM Ready (redundant): OK / NOK
- Beam Mode: 6 bits
- Beam Destination: 6 bits
- Beam Presence (crate 1A): YES / NO
- HV Presence (crate 1B): YES / NO

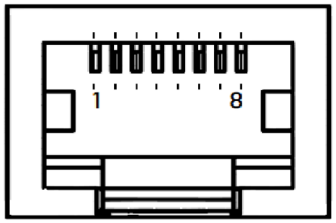
The FBIS uses this information to ensure that the BCM system has been configured for the correct beam and destination modes.

See **ESS-0105298** for more details

BCM – FBIS interface

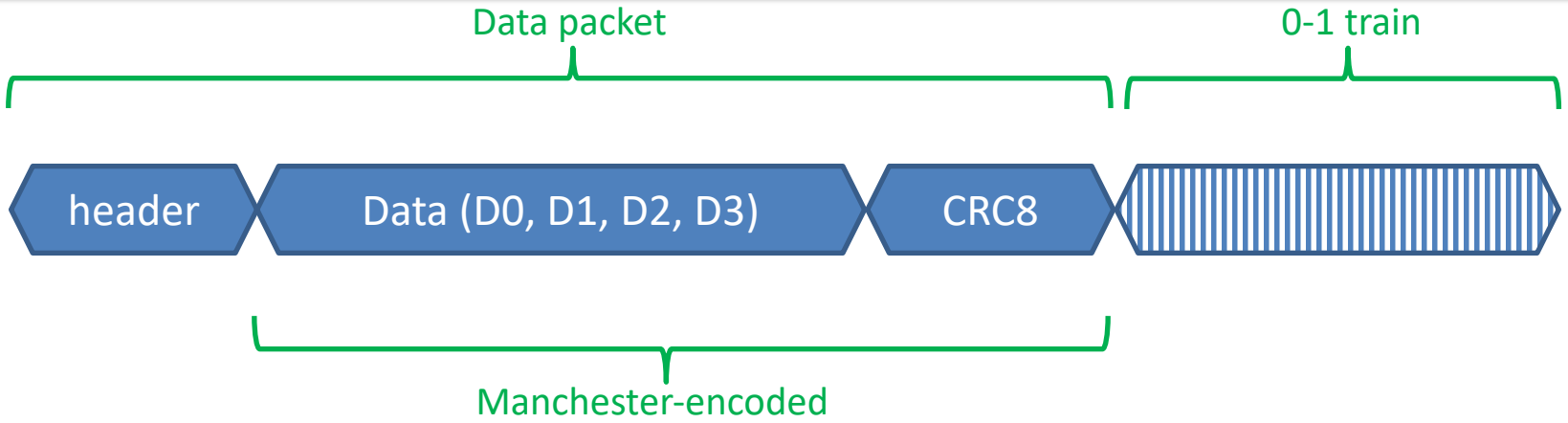
	BCM crates
RJ45 cable Pin Mapping	*1: Reserved*
	2: Reserved
	3: ACCT Beam Permit P
	4: ACCT Ready signal P
	5: ACCT Ready signal N
	6: ACCT Beam Permit N
	7: ACCT Serial Datalink P
	8: ACCT Serial Datalink N
	Housing: Shield

Beam Permit and BCM Ready are discrete signals



The RJ-45 OUT port on the SIS8300-KU provides 4 LVDS channels.

Serial data link – packet structure (draft)



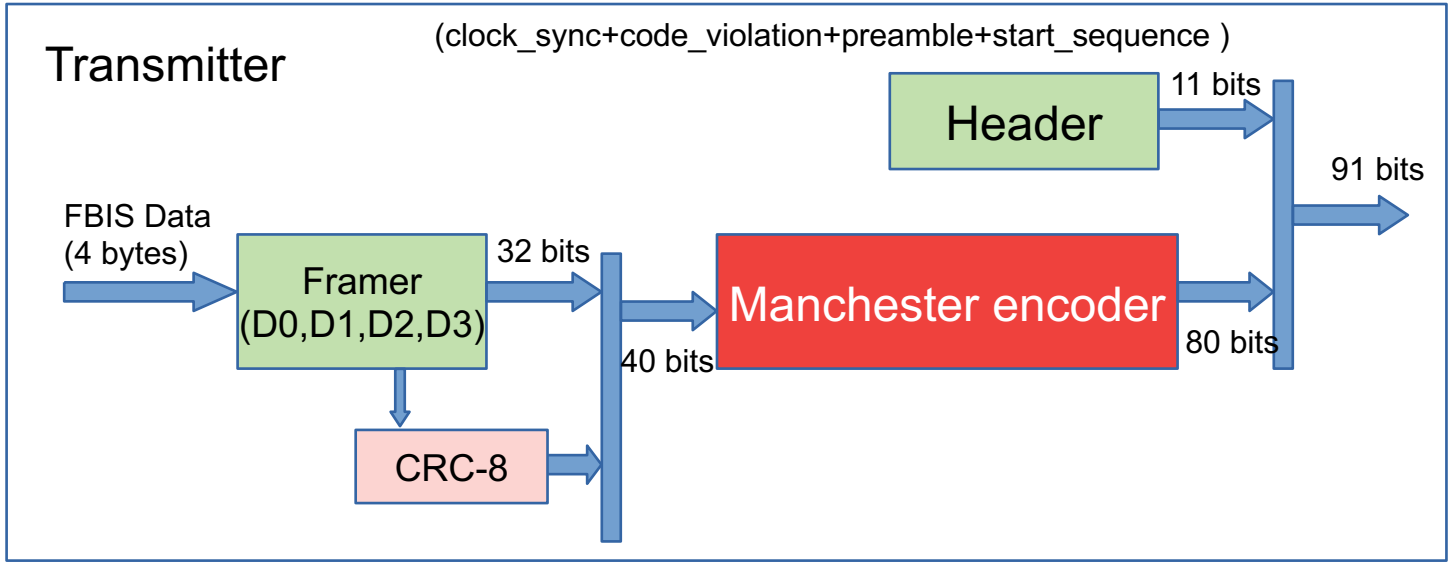
D0:	Beam Permit, BCM Ready
D1:	Beam Destination
D2:	Beam Mode
D3:	Beam presence, HV presence

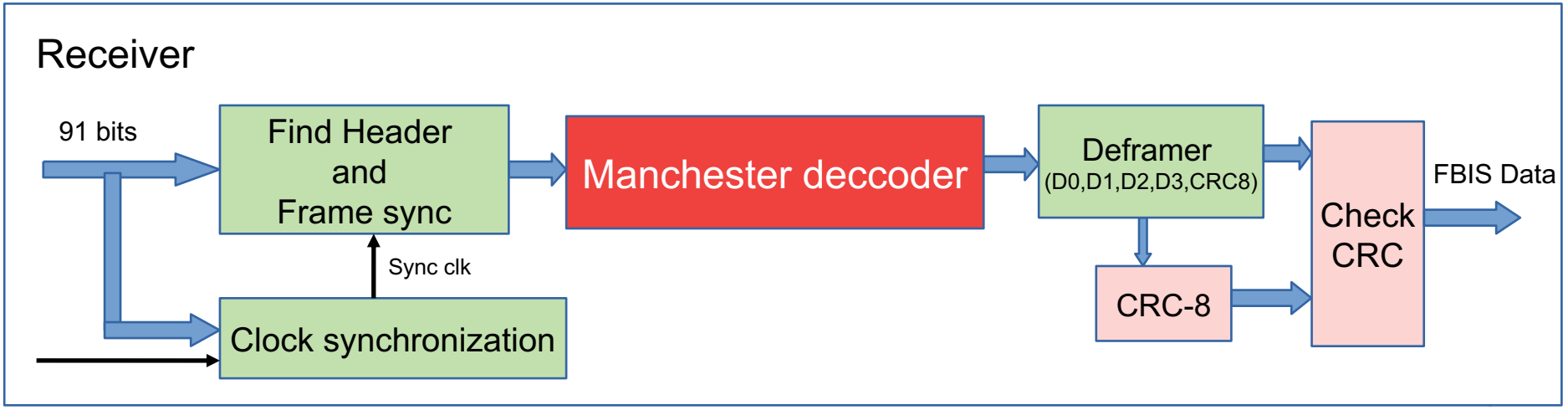
DC-balance is provided by:

- D0-D3 and CRC bytes are Manchester encoded
- A balanced train of 0-1 is sent in between each 2 consecutive packets
- The Header has the same number of 0 and 1 bits

Serial data link – FPGA implementation

- Line driver: LVDS
- Line rate: 11 Mbps
- Line encoding: Manchester
- Error detection: CRC-8
- Ref clock: 8 * bitrate

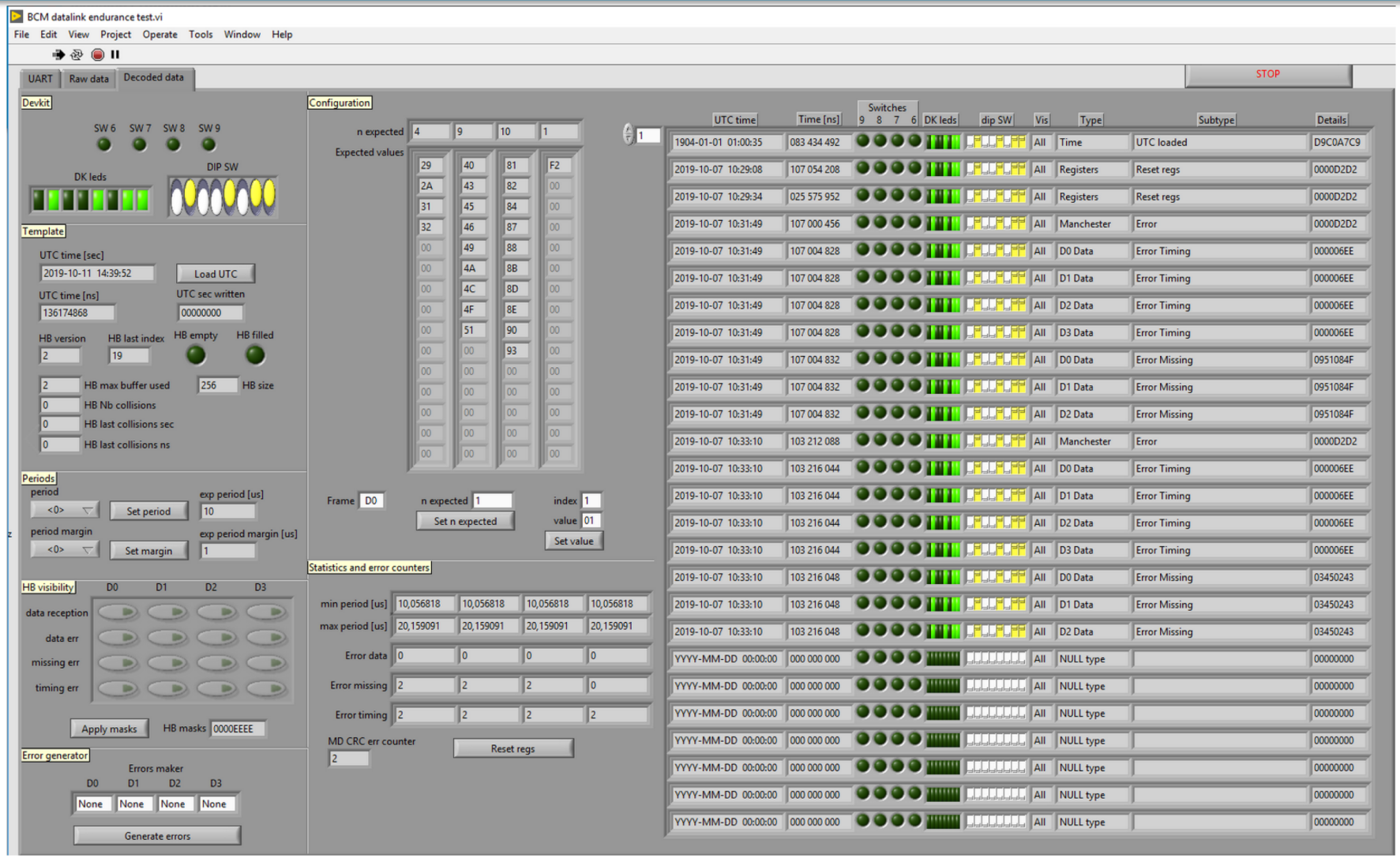




Endurance tests of the BCM-FBIS interface

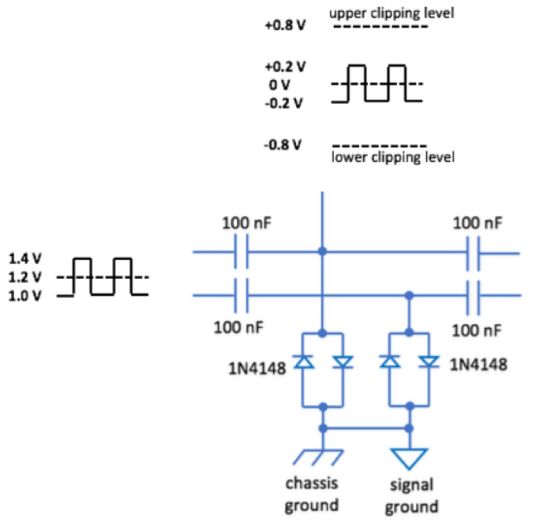
- The BCM and FBIS crates are hosted by two separate rack with a cable distance of ~20 m.
- The BCM electronics sends a data packet to a prototype FBIS every 10 us.
- BEAM_PERMIT and BCM_READY values are toggled and the BEAM_MODE and BEAM_DESTINATION values are incremented in each packet.
- A tester application is being used at the FBIS side for decoding the packets and measuring packet error rates.
- After 100 hours of run (i.e. 36 billion packets) in a 'quiet' environment, 2 CRC errors were detected.
- An LVDS protection module has also been developed with a prototype being used in the datalink tests.

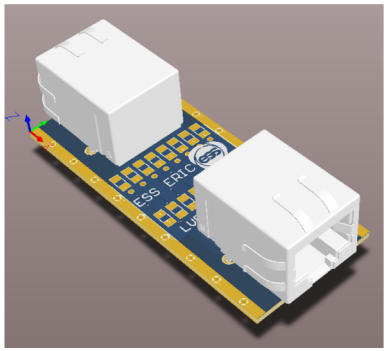
On-site tests of the BCM-FBIS datalink

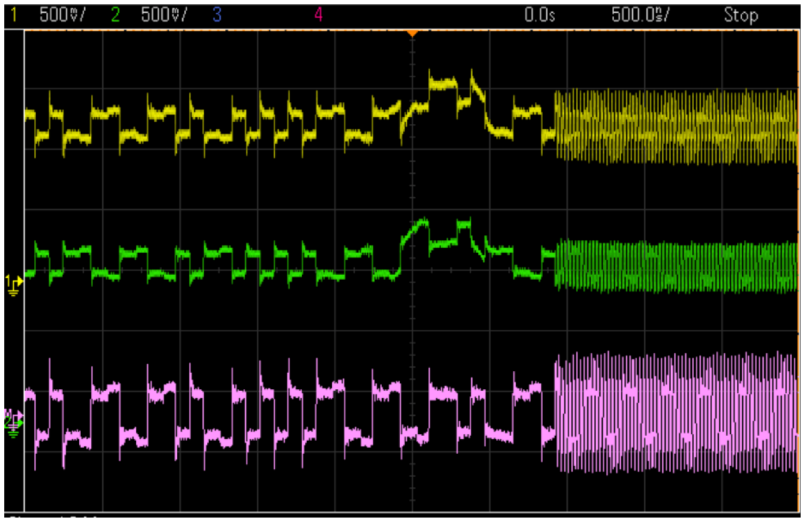


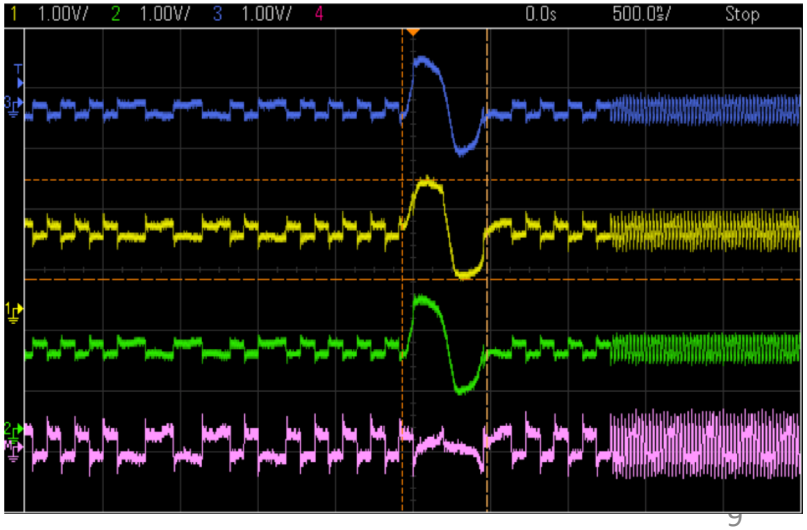
BCM-FBIS tester application developed by: Stephane Gabourin, ESS-MPS

Protection module for the BCM-FBIS interface









The protection module protects the LVDS buffers against DC currents and too-high / too-low voltages.

Forward Error Correction (FEC)

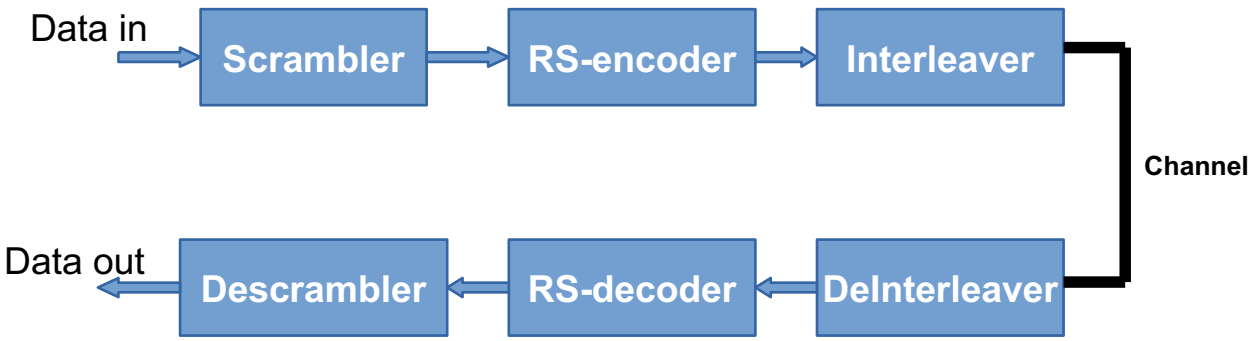
FEC using Reed Solomon codes is being studied as future improvement

Reed Solomon

- A powerful burst error correcting code
- The Reed-Solomon encoder takes a block of digital data and adds extra "redundant" bits.
- The advantage of using Reed-Solomon codes is that the probability of an error remaining in the decoded data is (usually) much lower than the probability of an error if Reed-Solomon is not used. This is often described as coding gain.

Interleaver

- Makes forward error correction more robust with respect to burst errors.

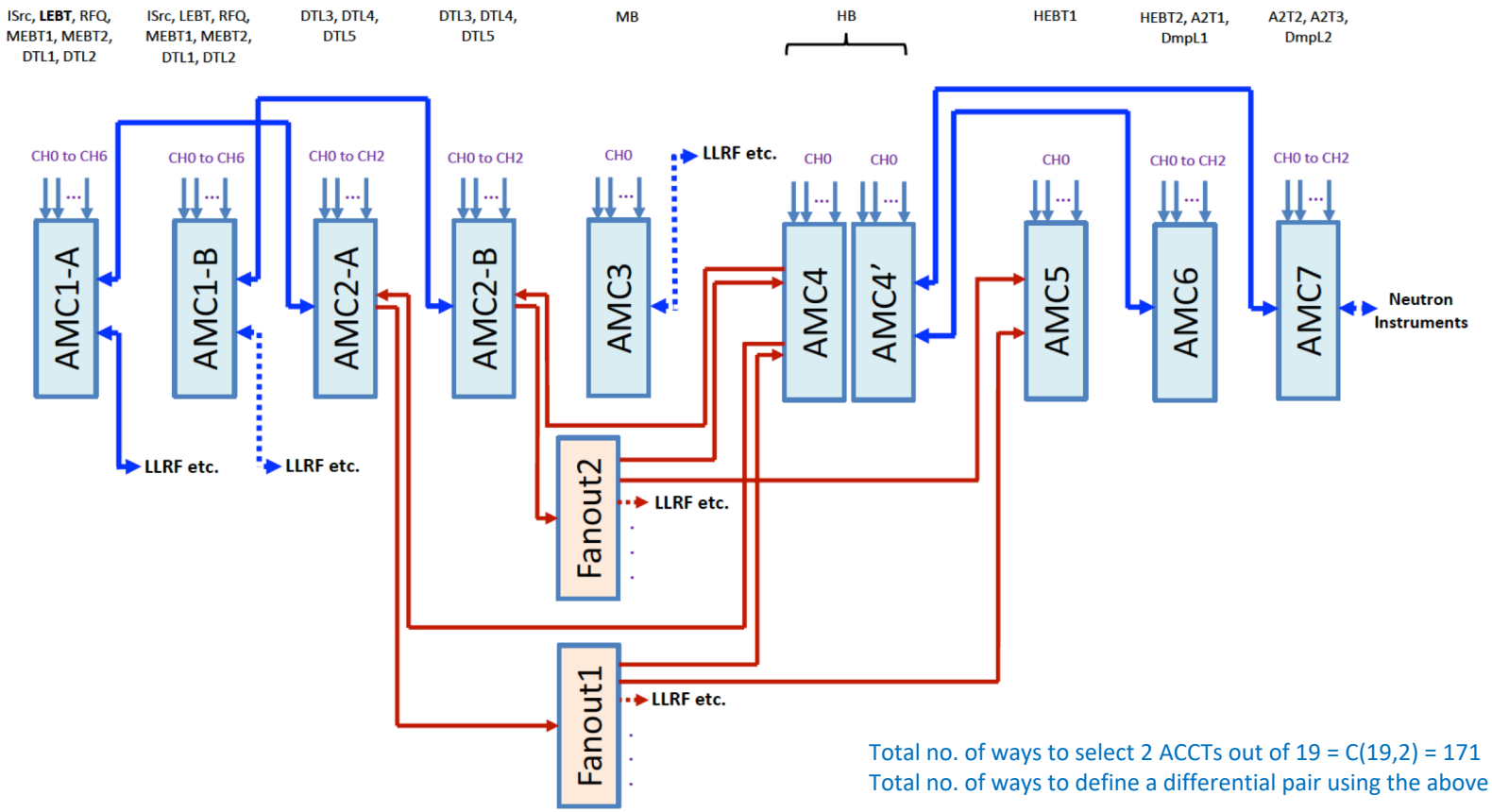


The optical link

Optical link use cases for the BCM system include:

- Sending BCM data to a downstream crate for differential current measurements
- Sending BCM data to other systems such as LLRF and Neutron Instruments
- Receiving beam data from other systems ex. FC for comparisions against BCM data
- Future upgrade of the BCM-FBIS interface

BCM optical cabling diagram

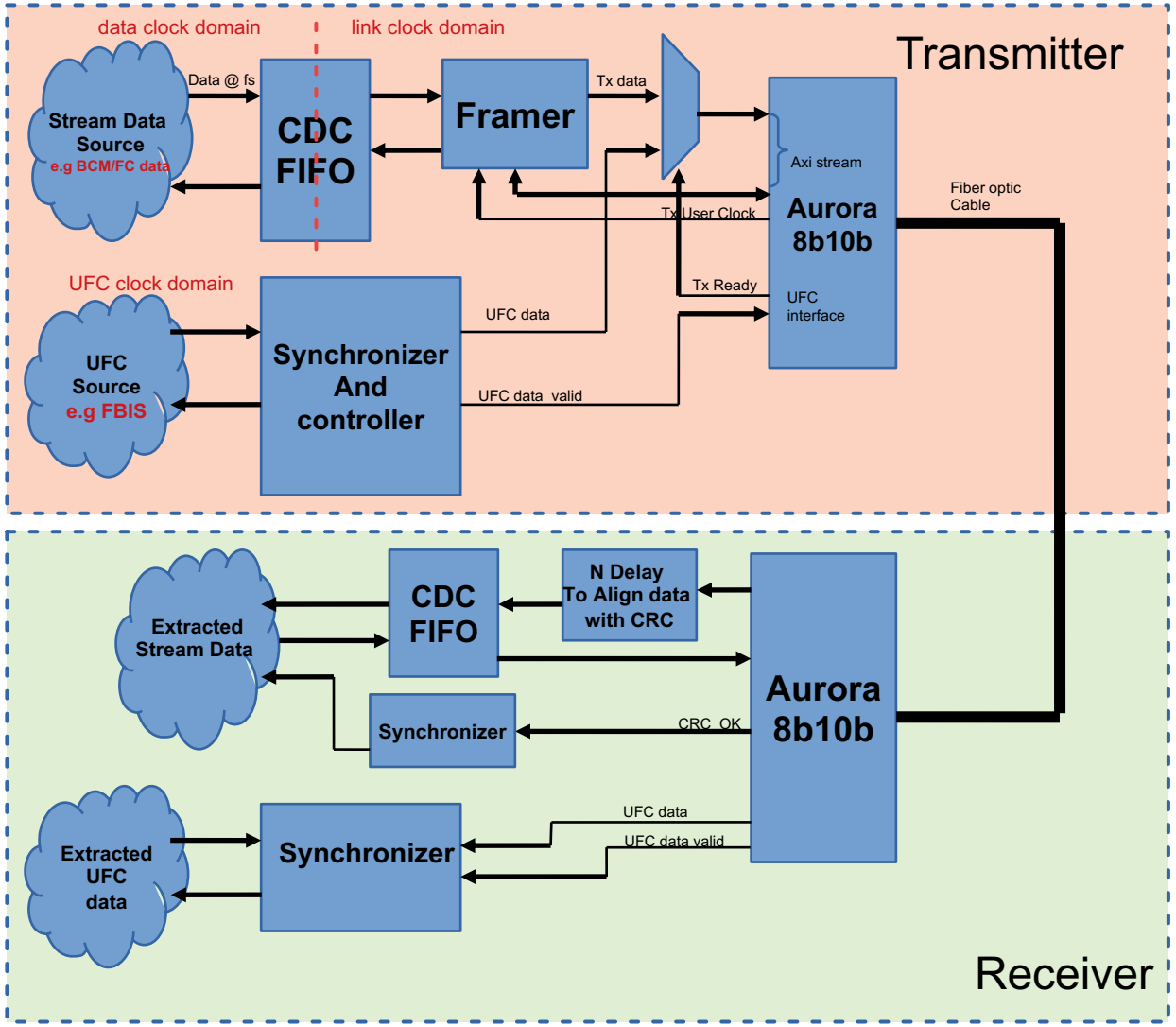


Total no. of ways to select 2 ACCTs out of 19 = C(19,2) = 171
Total no. of ways to define a differential pair using the above scheme = 57

↔ ⇠⇢	Full-duplex transmission using 'twin' optical cable
→ ⇢	Full-duplex transmission using 'single' optical cable
A	Main crate
B	Redundant crate
'	Extra AMC hosted by the same crate

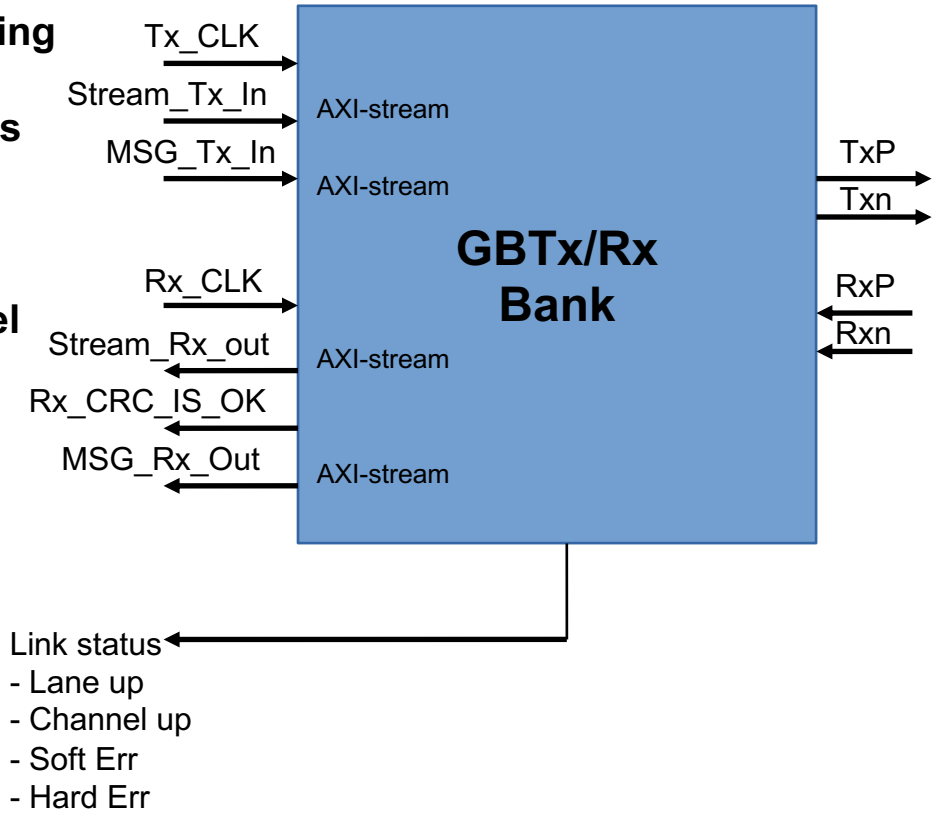
GBTx / Rx block diagram

- **Transmitter**
  - Transfer a stream 16-bits data @ fs<125 Msps
  - CDC FIFO for synchronization between data source clock domain and link user clock domain
  - Framer: make a frame from stream data. Length of frame : 10 samples
  - Transfer high priority 16-bits message
  - Rate of Msg < rate of stream data/10.
  - Synchronizer and controller to give interrupt to Aurora for transfer Msg over the link.
  - Msg can have own application layer protocol in order to transfer a packet with an error detection method.
  - CRC-32 just works for stream data
- **Receiver**
  - Rx EQ/Rx DFE/CDR done inside of Aurora
  - CRC is checked inside of Aurora
  - N delay in order to align data frame with crc ok signal
  - CDC fifo for synchronizing extracted data and CRC with user space clock domain
  - Msg data is directly extracted by Aurora just needs to be synchronized with the user domain clock



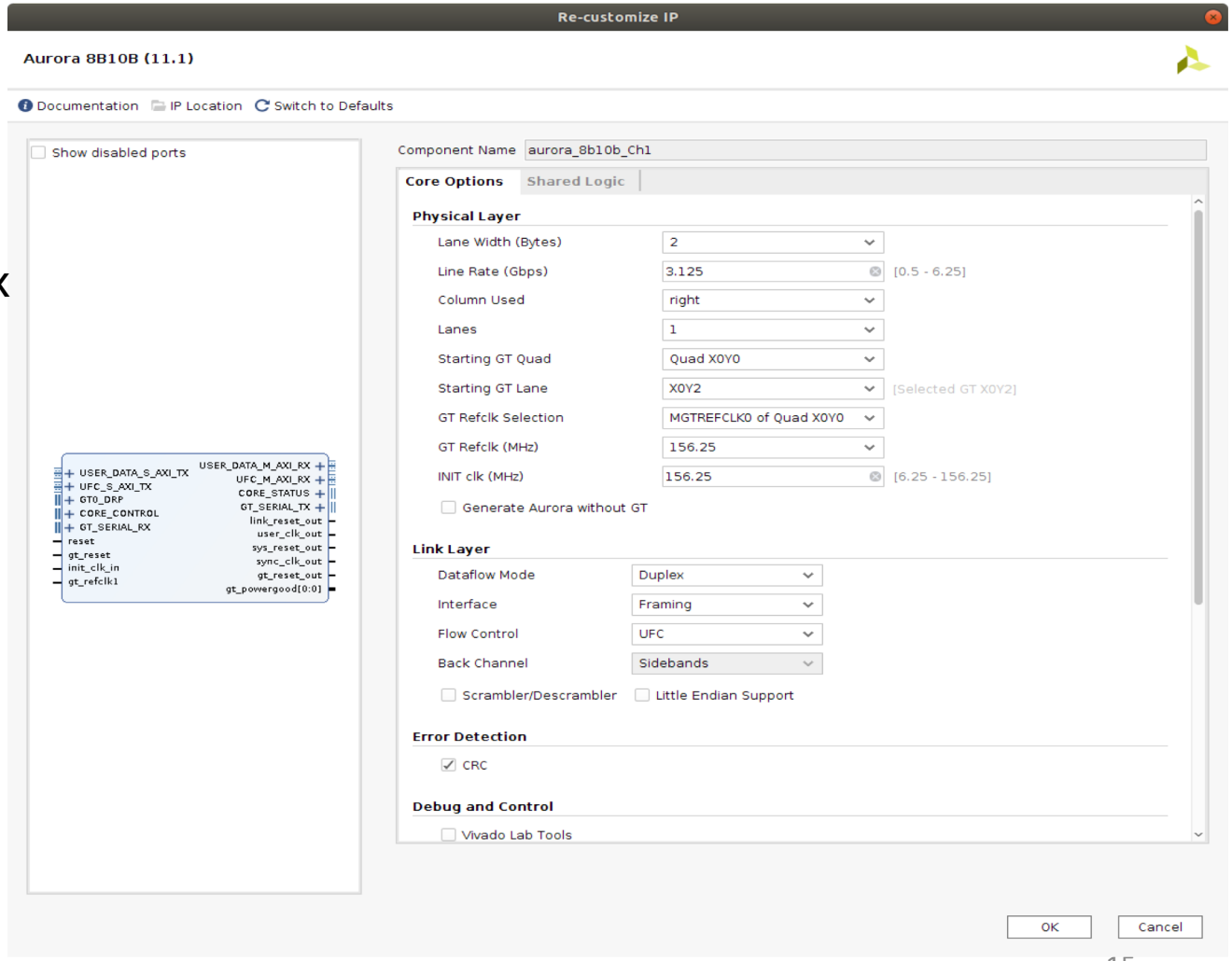
Low latency link IP bank

- **Giga Transceiver IP @ 3.125 Gbps with encoding**
- **Aurora 8b10b IP core**
- **Tx and Rx 16-bits stream data @ fs < 125 Msps**
- **Transfer and receive a 16 bits Msg**
- **CRC-32bits Error check**
- **Detect channel and lane Error**
- **Ability of recovering the link after lane/channel error detection**



Aurora configuration

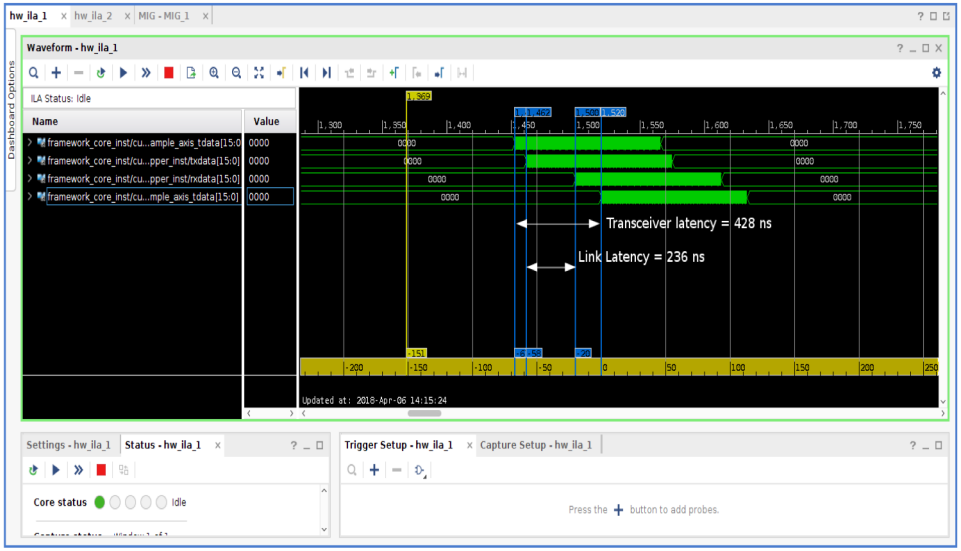
- Lane width: 2 byte
- Line Rate: 3.125 Gbps
- Lanes: 2
- Refclk: 156.25 MHz
- Dataflow Mode: Duplex
- Interface: Framing
- Flow control: UFC
- Error Detection: CRC



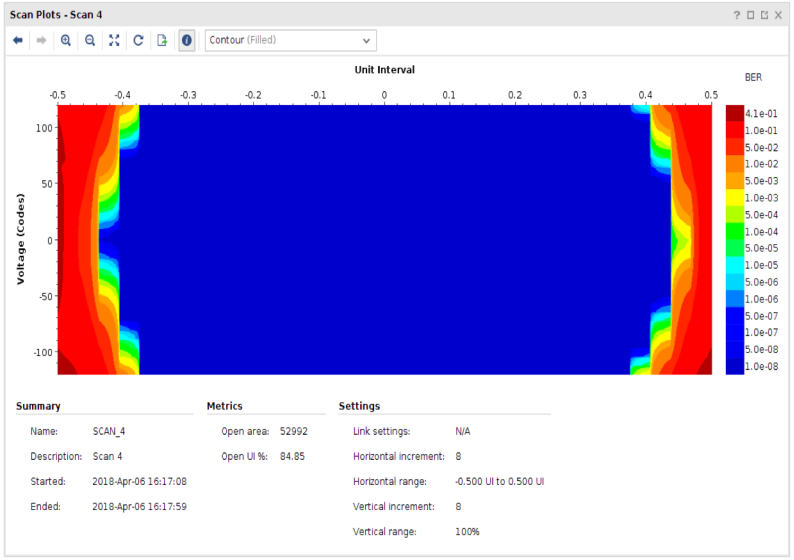
Performance analysis of a 3.125 Gbps optical link on the SIS8300-KU

EUROPEAN SPALLATION SOURCE

Line rate: 3.125 Gbps
IP core: Aurora 8b/10b



Latency of the optical link transceiver based on Aurora 8b/10b Xilinx IP core



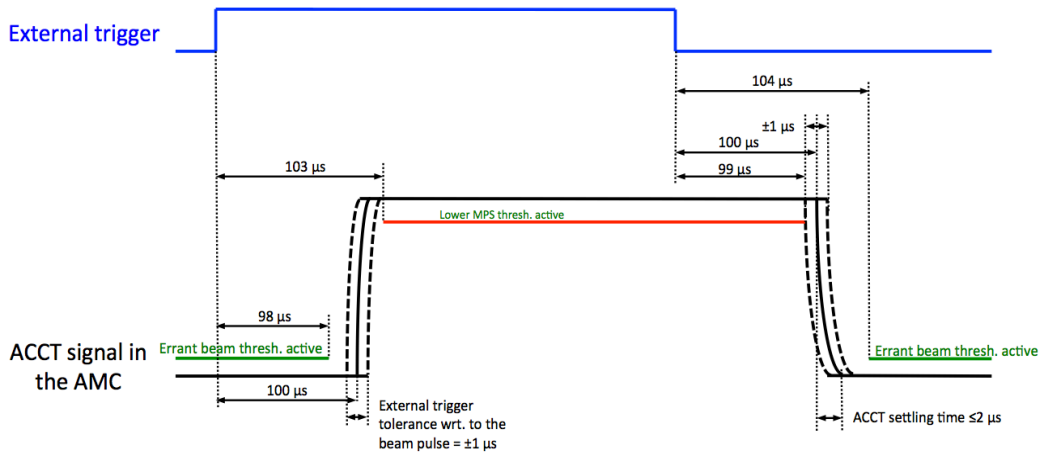
The EYE diagram on a SFP port

- **Data path latency without CRC detection: 428 ns**
- **Bit error rate: < 2e-15.**

BCM timing requirements

1. ADC clock (from EVR over backplane): 88.0525 MHz, locked to RF

2. Pulse trigger (from EVR over backplane): same width and frequency as the beam pulse; should be received by the BCM FPGA 100 us before the beam pulse.



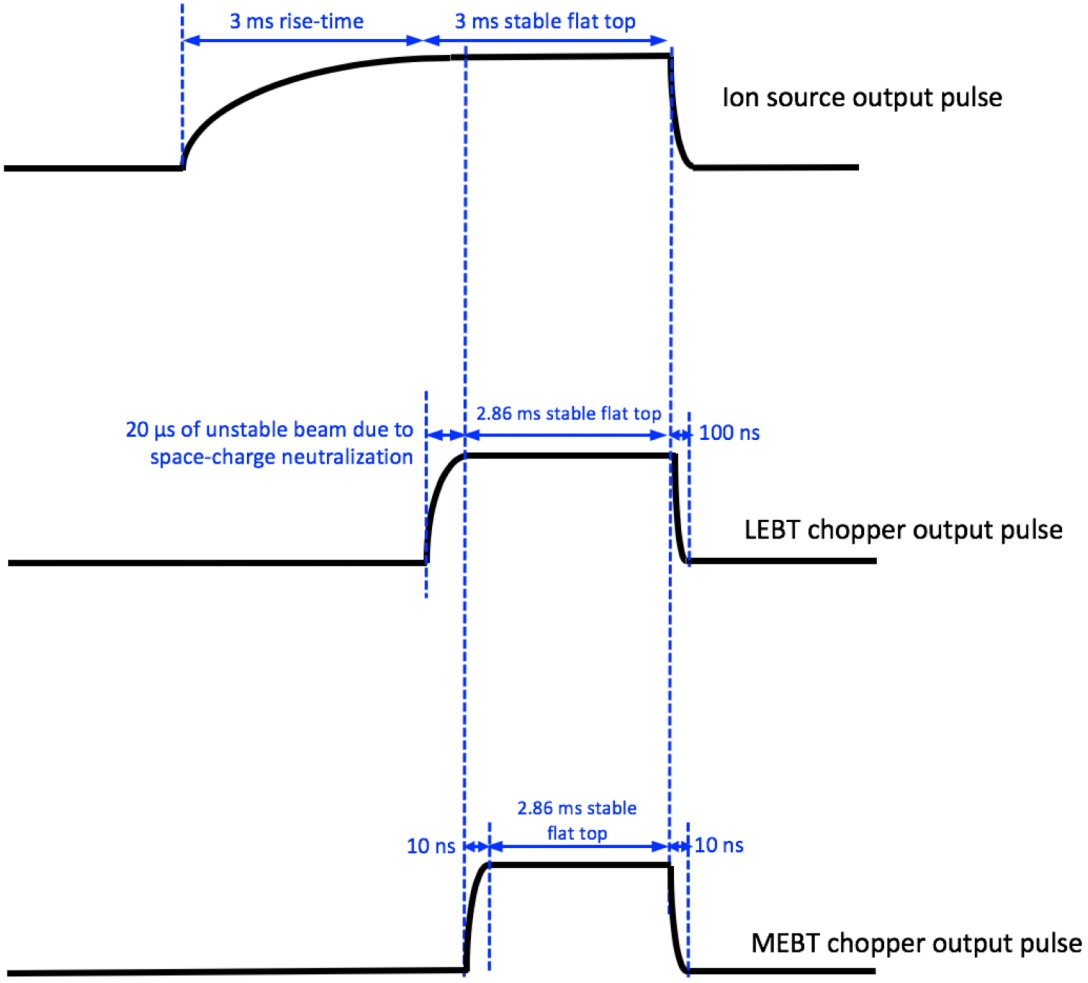
3. Beam mode: pulse current, width and repetition rate; upon changing to a new beam mode, the BCM FW reads/sets new MPS thresholds corresponding to that mode (lookup table in the FPGA); mode no. and definition based on **ESS-0038258**

4. Beam destination mode: beam destination

5. Calibration announcement: ACCT auto calibration starts at a well-defined time after receiving the announcement.

Pulse width changes from the ISrc to the MEBT

The ISrc, LEBT and MEBT pulses have different lengths and this will require 3 triggers with different lengths / timing for the BCM FW.



Summary / next steps

- BCM-FBIS interface has been discussed and agreed with the MPS group (little changes may still happen).
- Endurance tests with the final BCM electronics, final CAT-6A cable and a prototype FBIS are ongoing in the FEB.
- An LVDS protection module has been developed for the BCM-FBIS interface with a prototype being currently used in the tests.
- FEC and Reed-Solomon is being studied as a future upgrade.
- The optical link has successfully been used for testing the differential alarms.
- Adding FBIS data to the optical link is being studied as a future upgrade of the BCM-FBIS interface.