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# Low latency link development and MPS interface

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on behalf of:

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Background

BCM system has 3 special interfaces to external systems:

- BCM-FBIS interface: LVDS port on the SIS8300-KU
- Optical interface for sending BCM data to other crates: SFP port on the SIS8300-KU
- Timing:
   From EVR over the crate backplane







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The BCM system sends the following signals to the FBIS:

- Beam Permit (redundant):
- BCM Ready (redundant):
- Beam Mode:
- Beam Destination:
- Beam Presence (crate 1A):
- HV Presence (crate 1B):

OK / NOK OK / NOK 6 bits 6 bits YES / NO YES / NO

The FBIS uses this information to ensure that the BCM system has been configured for the correct beam and destination modes.

## BCM – FBIS interface



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	BCM crates	
RJ45 cable	1: Reserved	
Pin Mapping	2: Reserved	
	3: ACCT Beam Permit P	1
	4: ACCT Ready signal P	Beam Permit and BCM
	5: ACCT Ready signal N	Ready are discrete signals
	6: ACCT Beam Permit N	
	7: ACCT Serial Datalink P	
	8: ACCT Serial Datalink N	
	Housing: Shield	



The RJ-45 OUT port on the SIS8300-KU provides 4 LVDS channels.



D3: Beam presence, HV presence

DC-balance is provided by:

- D0-D3 and CRC bytes are Manchester encoded
- A balanced train of 0-1 is sent in between each 2 consecutive packets
- The Header has the same number of 0 and 1 bits

# Serial data link – FPGA implementation



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# Endurance tests of the BCM-FBIS interface

- The BCM and FBIS crates are hosted by two separate rack with a cable distance of ~20 m.
- The BCM electronics sends a data packet to a prototype FBIS every 10 us.
- BEAM\_PERMIT and BCM\_READY values are toggled and the BEAM\_MODE and BEAM\_DESTINATION values are incremented in each packet.
- A tester application is being used at the FBIS side for decoding the packets and measuring packet error rates.
- After 100 hours of run (i.e. 36 billion packets) in a 'quiet' environment, 2 CRC errors were detected.
- An LVDS protection module has also been developed with a prototype being used in the datalink tests.







### On-site tests of the BCM-FBIS datalink

	BCM datalink endurance test.vi								
Note Sub         Sub         Sub           Sub<	File Edit View Project Operate Tools Window Help								
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Perform       Desire	UART Raw data Decoded data								STOP
00.6       90.7       00.4       90.9       0.1       0.0       <	Devkit	Configuration				Switches			
Dick         Departs inter         Dick         Dick <thdick< th="">         Dick         Dick</thdick<>	SW 6 SW 7 SW 8 SW 9	n expected 4 9 10 1	A .	UTC time	Time [ns]	9 8 7 6 DK leds dip SW	Vis Type	Subtype	Details
K.kf.         DP W         J         J         F         A         F<		Expected values		1904-01-01 01:00:35	083 434 492	0000	All Time	UTC loaded	D9C0A7C9
A         A         A         A         A         A         B         A         B	DIP SW	29 40 81 F2		2019-10-07 10:29:08	107 054 208		All Registers	Reset regs	0000D2D2
Tensisti         Discussion         Discussion <thdiscussion< th="">         Discussion         Discussion</thdiscussion<>		2A 43 82 00 31 45 84 00		2019-10-07 10:29:34	025 575 952		All Registers	Reset regs	0000D2D2
Ufferented:       00       40       00	Template	32 46 87 00		2019-10-07 10:31:49	107 000 456		All Manchester	Error	0000D2D2
Product	UTC time [sec]	00 49 88 00		2019-10-07 10:31:49	107 004 828	<b>0000       </b>	All D0 Data	Error Timing	000006EE
No.         No. <td>2019-10-11 14:39:52 Load UTC</td> <td>00 4A 8B 00 1</td> <td></td> <td>2019-10-07 10:31:49</td> <td>107 004 828</td> <td><b>0000       </b>                           </td> <td>All D1 Data</td> <td>Error Timing</td> <td>000006EE</td>	2019-10-11 14:39:52 Load UTC	00 4A 8B 00 1		2019-10-07 10:31:49	107 004 828	<b>0000       </b>	All D1 Data	Error Timing	000006EE
HB version       HB version       HB version       NB version       Sign 0       <	UTC time [ns] UTC sec written 136174868 0000000	00 4F 8E 00		2019-10-07 10:31:49	107 004 828	••••	All D2 Data	Error Timing	000006EE
2         9         0	HB version HB last index HB empty HB filled	00 51 90 00		2019-10-07 10:31:49	107 004 828	0000 <b>III</b>	All D3 Data	Error Timing	000006EE
2       H6 max buffer ured 0       25       H6 size 0       M 0	2 19 🕥 🌑			2019-10-07 10:31:49	107 004 832		All D0 Data	Error Missing	0951084F
0       HB No collisions sc       0	2 HB max buffer used 256 HB size			2019-10-07 10:31:49	107 004 832	0000 <u>INI</u>	All D1 Data	Error Missing	0951084F
0       H0 AB Lot Collisions ns         0       HB Lot Collisions ns         0       D         0       D         1       D         0       D         1       D         0       D         0       D         0       D         0       D         0       D         0       D         0       D         0       D         0       D         0       D       D         0       D       D         0       D       D       D         0       D       D       D         0       D       D       D       D         0       D       D       D       D       D         0       D       D       D       D       D         0       D	0 HB Nb collisions			2019-10-07 10:31:49	107 004 832	<b>0000       </b>	All D2 Data	Error Missing	0951084F
Period exp period [us]   period margin   set period   10   set margin   min period lus   0.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818   10.055818 <td>0 HB last collisions ns</td> <td></td> <td></td> <td>2019-10-07 10:33:10</td> <td>103 212 088</td> <td></td> <td>All Manchester</td> <td>Error</td> <td>0000D2D2</td>	0 HB last collisions ns			2019-10-07 10:33:10	103 212 088		All Manchester	Error	0000D2D2
period exp period 10   period 10 1   period 10   exp period 10	Periods			2019-10-07 10:33:10	103 216 044	••••	All D0 Data	Error Timing	000006EE
COS       Set period       10       Error Timing       Set nexpected       value       1         Period margin       exp period margin       exp period margin       Set nexpected       value       1       1       2       1       1       2       1       1       2       1       1       2       1       1       2       1       1       2       1       1       2       1       1       2       1       1       2       1       1       2       1       1       2       1	period [us]	Frame D0 n expected 1 index	1	2019-10-07 10:33:10	103 216 044	•••• <b>•</b> •••	All D1 Data	Error Timing	000006EE
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data err missing err timing err       max period [us]       20,159091 <td>data reception</td> <td>min period [us] 10,056818 10,056818 10,056818</td> <td>10,056818</td> <td>2019-10-07 10:33:10</td> <td>103 216 048</td> <td>0000 <mark>IIII</mark></td> <td>All D1 Data</td> <td>Error Missing</td> <td>03450243</td>	data reception	min period [us] 10,056818 10,056818 10,056818	10,056818	2019-10-07 10:33:10	103 216 048	0000 <mark>IIII</mark>	All D1 Data	Error Missing	03450243
missing err timing err timing err       Error data       0<	data err	max period [us] 20,159091 20,159091 20,159091	20,159091	2019-10-07 10:33:10	103 216 048		All D2 Data	Error Missing	03450243
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Apply masks       HB masks 0000EEEE       Error timing       2       2       2       2       2       2       1       VYYY-MM-DD       0000000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 0000 000       000 0000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 000 000       000 00	timing err	Error missing 2 2 2	0	YYYY-MM-DD 00:00:00	000 000 000		All NULL type		00000000
Apply masks         HB masks         DOCRC err counter         Reset regs         VYYY-MM-DD         0000000         Image: Control of the set regs         MD CRC err counter         0000000         Image: Control of the set regs         Image: Contreg         Image: Control of the set regs<		Error timing 2 2 2	2	YYYY-MM-DD 00:00:00	000 000 000	••••	All NULL type		00000000
Error generator         2         None         All         NULL type         00000000           D0         D1         D2         D3         None	Apply masks HB masks 0000EEEE	MD CRC err counter Reset regs		YYYY-MM-DD 00:00:00	000 000 000		All NULL type		00000000
D0         D1         D2         D3           None         None         None         None         All         NULL type         00000000	Error generator Errors maker	2		YYYY-MM-DD 00:00:00	000 000 000	0000	All NULL type		00000000
	D0 D1 D2 D3			YYYY-MM-DD 00:00:00	000 000 000	0000	All NULL type		00000000
Openente errorr         Openente errorr         All         NULL type         00000000				YYYY-MM-DD 00:00:00	000 000 000		All NULL type		00000000

#### BCM-FBIS tester application developed by: Stephane Gabourin, ESS-MPS

# Protection module for the BCM-FBIS interface





The protection module protects the LVDS buffers against DC currents and too-high / too-low voltages.





## Forward Error Correction (FEC)



#### **Reed Solomon**

- A powerful burst error correcting code
- The Reed-Solomon encoder takes a block of digital data and adds extra "redundant" bits.
- The advantage of using Reed-Solomon codes is that the probability of an error remaining in the decoded data is (usually) much lower than the probability of an error if Reed-Solomon is not used. This is often described as coding gain.

#### Interleaver

• Makes forward error correction more robust with respect to burst errors.



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Optical link use cases for the BCM system include:

- Sending BCM data to a downstream crate for differential current measurements
- Sending BCM data to other systems such as LLRF and Neutron Instruments
- Receiving beam data from other systems ex. FC for comparisions against BCM data
- Future upgrade of the BCM-FBIS interface

## BCM optical cabling diagram





<b>+++ +++</b>	Full-duplex transmission using 'twin' optical cable
<b>→</b> ···· <b>&gt;</b>	Full-duplex transmission using 'single' optical cable
А	Main crate
В	Redundant crate
1	Extra AMC hosted by the same crate



## GBTx / Rx block diagram

#### Transmitter

- Transfer a stream 16-bits data @ fs<125 Msps</li>
- CDC FIFO for synchronization between data source clock domain and link user clock domain
- Framer: make a frame from stream data. Length of frame : 10 samples
- Transfer high priority 16-bits message
- Rate of Msg < rate of stream data/10.</li>
- Synchronizer and controller to give interrupt to Aurora for transfer Msg over the link.
- Msg can have own application layer protocol in order to transfer a packet with an error detection method.
- CRC-32 just works for stream data

#### Receiver

- Rx EQ/Rx DFE/CDR done inside of Aurora
- CRC is checked inside of Aurora
- N delay in order to align data frame with crc ok signal
- CDC fifo for synchronizing extracted data and CRC with user space clock domain
- Msg data is directly extracted by Aurora just needs to be synchronized with the user domain clock



## Low latency link IP bank



- Giga Transceiver IP @ 3.125 Gbps with encoding
- Aurora 8b10b IP core
- Tx and Rx 16-bits stream data @ fs < 125 Msps</li>
- Transfer and receive a 16 bits Msg
- CRC-32bits Error check
- Detect channel and lane Error
- Ability of recovering the link after lane/channel error detection



## Aurora configuration



- Lane width: 2 byte
- Line Rate: 3.125 Gbps
- Lanes: 2
- Refclk: 156.25 MHz
- Dataflow Mode: Duplex
- Interface: Framing
- Flow control: UFC
- Error Detection: CRC

	Re-custor	mize IP			8
Aurora 8B10B (11.1)					4
Documentation 📄 IP Location C Switch to Defaults	5				
Show disabled ports	Component Name aurora_8b10b_	_Ch1			
	Core Options Shared Logic				
	Physical Layer				î
	Lane Width (Bytes)	2	~		
	Line Rate (Gbps)	3.125	8	[0.5 - 6.25]	
	Column Used	right	~		- 11
	Lanes	1	~		
	Starting GT Quad	Quad X0Y0	~		
	Starting GT Lane	X0Y2	~	[Selected GT X0Y2]	
	GT Refclk Selection	MGTREFCLK0 of Quad X0Y0	o ~		
	GT Refclk (MHz)	156.25	~		
+ USER_DATA_S_AXI_TX USER_DATA_M_AXI_RX + + + UFC_S_AXI_TX UFC_M_AXI_RX + +	INIT clk (MHz)	156.25	$\otimes$	[6.25 - 156.25]	
I + GT0_DRP     CORE_STATUS +          I + CORE_CONTROL     GT_SERIAL_TX +          I + GT_SERIAL_RX     link_reset_out -	Generate Aurora without GT				
reset user_clk_out = gt_reset sys_reset_out =	Link Layer				- 11
init_clk_in syn_clk_out gt_refclk1 gt_reset_out gt_refclk1 gt_reset_out	Dataflow Mode	Duplex 🗸			
g_powergood(oros)	Interface	Framing 🗸			
	Flow Control	UFC 🗸			
	Back Channel	Sidebands 🗸			
	Scrambler/Descrambler				
	Error Detection				
	CRC				
	Debug and Control				
	Vivado Lab Tools				~

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# Performance analysis of a 3.125 Gbps optical link on the SIS8300-KU



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4.1e-01

1.0e-01

5.0e-02

1.0e-02

5.0e-03

1.0e-03

.0e-04

1.0e-04

.0e-05

### Line rate: 3.125 Gbps IP core: Aurora 8b/10b



Latency of the optical link transceiver based on Aurora 8b/10b Xilinx IP core

The EYE diagram on a SFP port

- Data path latency without CRC detection: 428 ns
- Bit error rate:

< 2e-15.

## **BCM timing requirements**

- 1. ADC clock (from EVR over backplane): 88.0525 MHz, locked to RF
- 2. Pulse trigger (from EVR over backplane): same width and frequency as the beam pulse; should be received by the BCM FPGA 100 us before the beam pulse.



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- 3. Beam mode: pulse current, width and repetition rate; upon changing to a new beam mode, the BCM FW reads/sets new MPS thresholds corresponding to that mode (lookup table in the FPGA); mode no. and definition based on **ESS-0038258**
- 4. Beam destination mode: beam destination
- 5. Calibration announcement: ACCT auto calibration starts at a well-defined time after receiving the announcement.

# Pulse width changes from the ISrc to the MEBT



## Summary / next steps



- BCM-FBIS interface has been discussed and agreed with the MPS group (little changes may still happen).
- Endurance tests with the final BCM electronics, final CAT-6A cable and a prototype FBIS are ongoing in the FEB.
- An LVDS protection module has been developed for the BCM-FBIS interface with a prototype being currently used in the tests.
- FEC and Reed-Solomon is being studied as a future upgrade.
- The optical link has successfully been used for testing the differential alarms.
- Adding FBIS data to the optical link is being studied as a future upgrade of the BCM-FBIS interface.