

Behavioural Simulations

Rafał Kielbik

Issues to discuss

1. Potential tools (XSim / ModelSim / QuestaSim)
2. Compilation hierarchy
3. Simulation libraries
4. Testbench & stimuli

Potential tools (XSim / ModelSim / QuestaSim)

XSim

- + Built in Vivado (native)
- + No additional license required
- Lower efficiency
- No variables supported (in waveforms)

ModelSim / QuestaSim

- External tool (but integrated)
- Expensive license required
- + High simulation speed
- + All statements supported (e.g.: “case?”)

Compilation hierarchy

- Simulation Sources (6)
 - simulation (6)
 - Verilog Header (1)
 - tstbench**(top_tb) (top_tb.vhd) (1)
 - NIOBE_simenv_i : NIOBE_ifc1211_central_simenv(simenv) (NIOBE_ifc1211_central_simenv.vhd) (5)
 - top_fpga : top_IFC1211_CENTRAL_a0(rtl) (top_ifc1211_central_example_0_a0.vhd) (2)
 - top_phy.tosca2b_ip_i : tosca2b_niobe_ifc_central_ip01_fbi(rtl) (tosca2b_niobe_central_ip01_fbi.vhd) (7)
 - xuser_ex0_i : xuser_top(rtl) (xuser_top.vhd) (5)
 - n_blm_top_1 : n_blm_top(rtl) (n_blm_top.vhd) (108)
 - gpio_ifc1211_gpio_ifc1211_i : niobe_ifc1211_central_xuser_gpio_mgt(rtl) (niobe_ifc1211_central_xuser_gpio_gtx_mgt.vhd) (4)
 - inst_ad3110_fmc1 : ent_ad3110(arch) (ent_ad3110.vhd) (13)
 - inst_dummy_fmc2 : ent_empty_fmc(arch) (ent_empty.vhd) (2)
 - niobe_ifc1410_central_xuser_gpio_mgt(rtl) (niobe_ifc1410_central_xuser_gpio_gtx_mgt.vhd) (2)
 - gpio_tcsr_gpio_dpram_tmem_0 : xuser_gpio_tcsr_gpio_dpram_tmem_0(arch) (xuser_gpio_tcsr_gpio_dpram_tmem_0.vhd) (1)
 - gpio_tcsr_gpio_dpram_tmem_1 : xuser_gpio_tcsr_gpio_dpram_tmem_1(arch) (xuser_gpio_tcsr_gpio_dpram_tmem_1.vhd) (1)
 - emul_fmc1 : emul_ifc1211_fmc(emulate) (emul_ifc1211_fmc.vhd) (1)
 - emul_fmc2 : emul_ifc1211_fmc(emulate) (emul_ifc1211_fmc.vhd) (1)
 - emul_general : emul_ifc1211_general(emulate) (emul_ifc1211_general.vhd) (1)
 - emul_SMEM_12 : emul_ifc1211_smem_ddr3(emulate) (emul_ifc1211_smem_ddr3.vhd) (1)
 - smem_on.ddr3_0_i : ddr3_4g (ddr3_4g.v) (1)
 - smem_on.ddr3_1_i : ddr3_4g (ddr3_4g.v) (1)

- Testbench for IFC 1211 (prepared by IOxOS)
- Simulated: Tosca + DDR + XUser
- No ADCs (dummy data generators used)
- Speed: ~100 ns / 1 min

Compilation hierarchy

- Simulation Sources (6)
 - simulation (6)
 - Verilog Header (1)
 - tstbench**(top_tb) (top_tb.vhd) (1)
 - NIOBE_simenv_i : NIOBE_ifc1211_central_simenv(simenv) (NIOBE_ifc1211_c...)
 - top_fpga : top_IFC1211_CENTRAL_a0(rtl) (top_ifc1211_central_example...)
 - top_phy.tosca2b_ip_i : tosc2b_niobe_ifc_central_ip01_fbi(rtl) (tosca2b_niobe_central_ip01_fbi.vhd) (7)
 - xuser_ex0_i : xuser_top(rtl) (xuser_top.vhd) (5)
 - n_blm_top_1 : n_blm_top(rtl) (n_blm_top.vhd) (108)
 - gpio_ifc1211_gpio_ifc1211_i : niobe_ifc1211_central_xuser_gpio_mgt(rtl) (niobe_ifc1211_central_xuser_gpio_gtx_mgt.vhd) (4)
 - inst_ad3110_fmc1 : ent_ad3110(arch) (ent_ad3110.vhd) (13)
 - inst_dummy_fmc2 : ent_empty_fmc(arch) (ent_empty.vhd) (2)
 - niobe_ifc1410_central_xuser_gpio_mgt(rtl) (niobe_ifc1410_central_xuser_gpio_gtx_mgt.vhd) (2)
 - gpio_tcsr_gpio_dpram_tmem_0 : xuser_dpram_4Kx64 (xuser_dpram_4Kx64.xci)
 - gpio_tcsr_gpio_dpram_tmem_1 : xuser_dpram_4Kx64 (xuser_dpram_4Kx64.xci)
 - emul_fmc1 : emul_ifc1211_fmc(emulate) (emul_ifc1211_fmc.vhd)
 - emul_fmc2 : emul_ifc1211_fmc(emulate) (emul_ifc1211_fmc.vhd)
 - emul_general : emul_ifc1211_general(emulate) (emul_ifc1211_central_general.vhd)
 - emul_SMEM_12 : emul_ifc1211_smem_ddr3(emulate) (emul_ifc1211_smem_ddr3.vhd) (2)
 - smem_on.ddr3_0_i : ddr3_4g (ddr3_4g.v)
 - smem_on.ddr3_1_i : ddr3_4g (ddr3_4g.v)

Required files:

1. Project-specific sources
2. Tosca modules
3. XUser example testbenches

Compilation hierarchy

- Simulation Sources (6)
 - simulation (6)
 - Verilog Header (1)
 - tstbench(top_tb) (top_tb.vhd) (1)
 - NIOBE_simenv_i : NIOBE_ifc1211_central_simenv(simenv) (NIOBE_ifc1211_c...)
 - top_fpga : top_IFC1211_CENTRAL_a0(rtl) (top_ifc1211_central_example...)
 - top_phy.tosca2b_ip_i : toscab2b_niobe_ifc_central_ip01_fbi(rtl) (tosca2b_niobe_central_ip01_fbi.vhd) (7)

Required files:

1. Project-specific sources
2. Tosca modules
3. XUser example testbenches

```
add_sim_files_to_project.tcl - /home/rkielbik/work/Lodz_development/fw/prj/nBlm - Geany
File Edit Search View Document Project Build Tools Help

add_sim_files_to_project.tcl x
1 set_property SOURCE_SET sources [get_filesets simulation]
2
3 add_files -fileset simulation -norecurse modules/tosca2b/06_Simulation/20_sim_support/NIOBE_KU_simu_procedures.vhd
4 add_files -fileset simulation -norecurse fw/sim/tb/top_tb.vhd
5 add_files -fileset simulation -norecurse modules/xuser_example_0/06_Simulation/01_Environment/NIOBE_ifc1211_central_simenv.vhd
6 add_files -fileset simulation -norecurse modules/xuser_example_0/03_Src_top_ifc1211/top_ifc1211_central_example_0_a0.vhd
7 add_files -fileset simulation -norecurse modules/tosca2b/06_Simulation/02_Models/01_bfm_emul_ifc1211/03_Src/emul_ifc1211_fmc.vhd
8 add_files -fileset simulation -norecurse modules/tosca2b/06_Simulation/02_Models/01_bfm_emul_ifc1211/03_Src/emul_ifc1211_central_general.vhd
9 add_files -fileset simulation -norecurse modules/tosca2b/06_Simulation/02_Models/04_bfm_emul_smem_ddr2_3/03_Src/emul_ifc1211_smem_ddr3.vhd
10 add_files -fileset simulation -norecurse modules/tosca2b/06_Simulation/02_Models/04_bfm_emul_smem_ddr2_3/03_Src/ddr3_4g.v
11
12 set_property include_dirs modules/xuser_example_0/06_Simulation/06_ModelSIM [current_fileset]
13
14 set_property top tstbench [get_filesets simulation]
15 set_property top_lib xil defaultlib [get_filesets simulation]
16 update_compile_order -fileset simulation
17
```

Simulation script

```
rkielbik@brok:~/work/Lodz_development/fw/sim/scripts
File Edit View Search Terminal Help
[rkielbik@brok scripts]$ pwd
/home/rkielbik/work/Lodz_development/fw/sim/scripts
[rkielbik@brok scripts]$ cat Makefile
PRJ_NAME=nB1m

SIMULATOR=questa

SIMLIB_DIR=./kintexu_simlib
IP_DIR=./ip_dir
EXPORTED_SIM_DIR=./exported_sim
```

```
rkielbik@brok:~/work/Lodz_development/fw/sim/scripts
File Edit View Search Terminal Help
[rkielbik@brok scripts]$ pwd
/home/rkielbik/work/Lodz_development/fw/sim/scripts
[rkielbik@brok scripts]$ make

Usage:
    make [command]

Possible commands:
    compile_libs - generates simulation libraries
    export_ips   - exports IP sources for simulations
    export_sim   - generates simulation scrips
    set_files    - prepares auxiliary environment files

    compile     - compiles design simulation files
    elaborate   - opitmizes top module to be simulated
    simulate    - opens GUI and launches simulation

    clean_logs  - removes all log files created during simulations
    clean       - removes all files and folders created for simulations

    prepare_sim - compile_libs, export_ips
    run_sim     - clean_logs, export_sim, set_files, compile,
                 elaborate, simulate

[rkielbik@brok scripts]$
```

Testbench & stimuli

```
top_tb.vhd - /home/rkielbik/work/Lodz_development/fw/sim/tb - Geany
File Edit Search View Document Project Build Tools Help

top_tb.vhd x
491 | for i in 0 to cb_pkg.NUM_OF_CHANNELS-1 loop
492 |
493 |     bank_selector := std_logic_vector(to_unsigned(i,16));
494 |
495 |     if i = 0 then
496 |         base_addr(i) := BASE_PAGE_ADDR_0 & x"000";
497 |     else
498 |         base_addr(i) := end_addr(i-1);
499 |     end if;
500 |
501 |     end_addr(i) := std_logic_vector(unsigned(base_addr(i)) + cb_pkg.BURST_MULTIPLIER * cb_pkg.BURST_BOUNDARY);
502 |     burst_size(i) := x"0000" & BURST_SIZE_256;
503 |     data_interrupt_threshold(i) := std_logic_vector((unsigned(end_addr(i)) - unsigned(base_addr(i))) / 2);
504 |     latency_threshold(i) := x"0000" & x"0004";           -- 4 ms
505 |     generator_parameters(i) := x"00" & x"000000";       -- rate: 0/0 - data generator disabled
506 |     sample_threshold(i) := x"0000" & x"01F0";
507 |
508 |     -- base_addr
509 |     reg_selector := std_logic_vector(to_unsigned(xuser_tcsr_pkg.REG_BASE_ADDR,16));
510 |     IO_WRITE_RQ ("B_104_001", PCIE_0_BFM, cbrs_addr , X"F", bank_selector & reg_selector);      wait for TIME_FOR_REGISTER_OPERATION;
511 |     IO_WRITE_RQ ("B_104_001", PCIE_0_BFM, cbrv_addr , X"F", base_addr(i));                  wait for TIME_FOR_REGISTER_OPERATION;
512 |
513 |     -- end_addr
514 |     reg_selector := std_logic_vector(to_unsigned(xuser_tcsr_pkg.REG_END_ADDR,16));
515 |     IO_WRITE_RQ ("B_104_001", PCIE_0_BFM, cbrs_addr , X"F", bank_selector & reg_selector);      wait for TIME_FOR_REGISTER_OPERATION;
516 |     IO_WRITE_RQ ("B_104_001", PCIE_0_BFM, cbrv_addr , X"F", end_addr(i));                  wait for TIME_FOR_REGISTER_OPERATION;
517 |
518 |     -- burst_size
519 |     reg_selector := std_logic_vector(to_unsigned(xuser_tcsr_pkg.REG_BURST_SIZE,16));
520 |     IO_WRITE_RQ ("B_104_001", PCIE_0_BFM, cbrs_addr , X"F", bank_selector & reg_selector);      wait for TIME_FOR_REGISTER_OPERATION;
521 |     IO_WRITE_RQ ("B_104_001", PCIE_0_BFM, cbrv_addr , X"F", burst_size(i));                wait for TIME_FOR_REGISTER_OPERATION;
522 |
```


To do

1. Implement adding simulation sources in Makefile
2. Adapt stimuli to current configuration registers
3. Extend testbench (e.g. with models of new modules to be designed)