Behavioural Simulations

Rafał Kiełbik

Issues to discuss

1. Potential tools (XSim / ModelSim / QuestaSim)
2. Compilation hierarchy
3. Simulation libraries
4. Testbench & stimuli

Potential tools (XSim / ModelSim / QuestaSim)

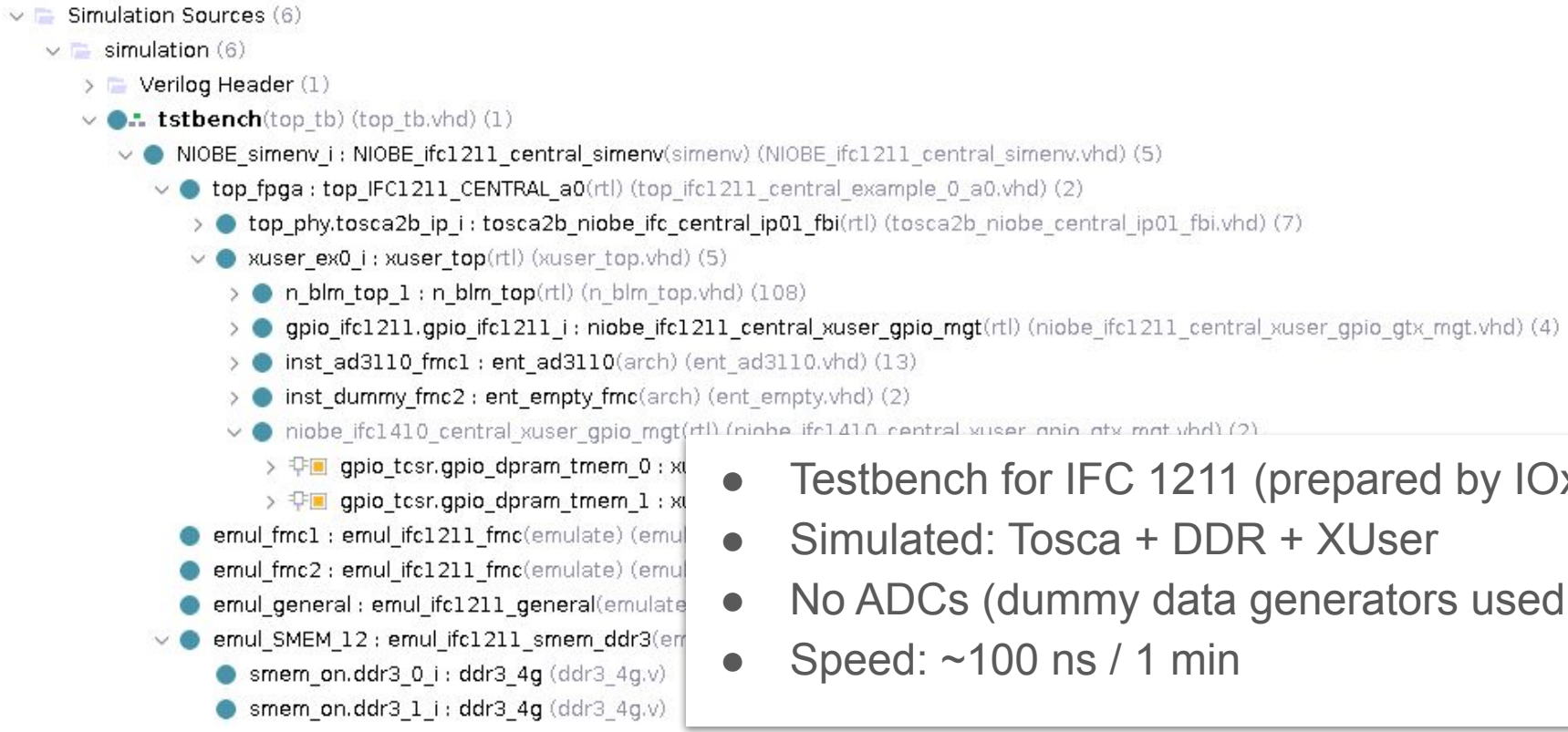
XSim

+ Built in Vivado (native)
+ No additional license required
- Lower efficiency
- No variables supported (in waveforms)

ModelSim / QuestaSim

- External tool (but integrated)
- Expensive license required
+ High simulation speed
+ All statements supported (e.g.: “case?”)

Compilation hierarchy



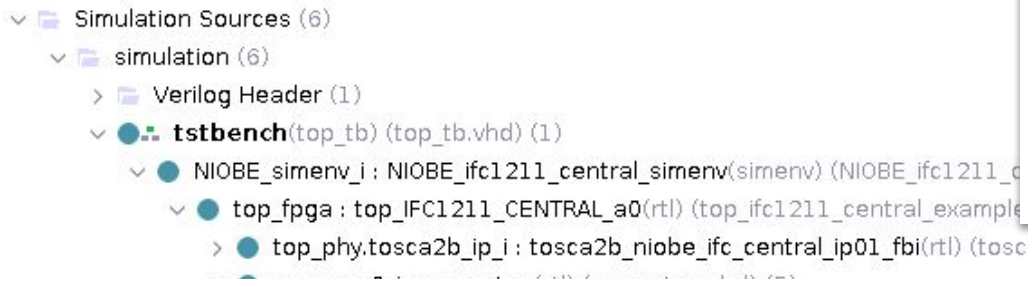
- Testbench for IFC 1211 (prepared by IOxOS)
- Simulated: Tosca + DDR + XUser
- No ADCs (dummy data generators used)
- Speed: ~100 ns / 1 min

Compilation hierarchy

Required files:

1. Project-specific sources
2. Tosca modules
3. XUser example testbenches

Compilation hierarchy



Required files:

1. Project-specific sources
2. Tosca modules
3. XUser example testbenches

add_sim_files_to_project.tcl - /home/rkielbik/work/Lodz_development/fw/prj/nBlm - Geany

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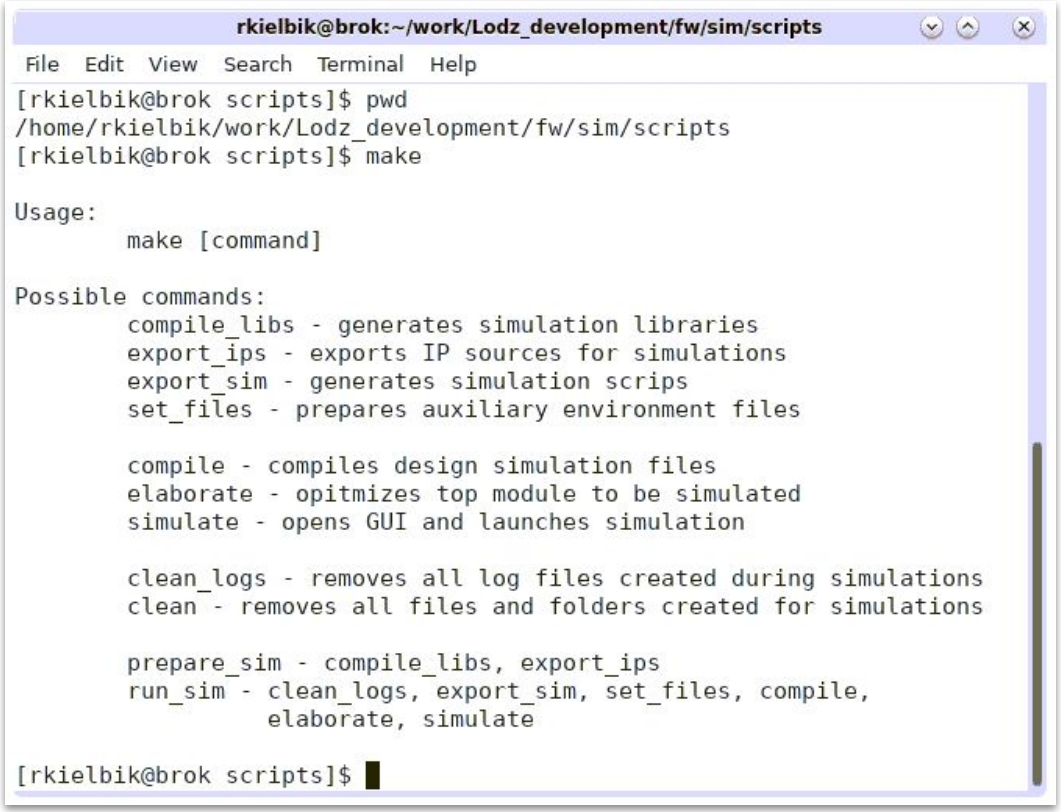
add_sim_files_to_project.tcl

```
1  set_property SOURCE_SET sources [get_filesets simulation]
2
3  add_files -fileset simulation -norecurse modules/tosca2b/06_Simulation/20_sim_support/NIOBE_KU_simu_procedures.vhd
4  add_files -fileset simulation -norecurse fw/sim/tb/top_tb.vhd
5  add_files -fileset simulation -norecurse modules/xuser_example_0/06_Simulation/01_Environment/NIOBE_ifc1211_central_simenv.vhd
6  add_files -fileset simulation -norecurse modules/xuser_example_0/03_Src_top_ifc1211/top_ifc1211_central_example_0_a0.vhd
7  add_files -fileset simulation -norecurse modules/tosca2b/06_Simulation/02_Models/01_bfm_emul_ifc1211/03_Src/emul_ifc1211_fmc.vhd
8  add_files -fileset simulation -norecurse modules/tosca2b/06_Simulation/02_Models/01_bfm_emul_ifc1211/03_Src/emul_ifc1211_central_general.vhd
9  add_files -fileset simulation -norecurse modules/tosca2b/06_Simulation/02_Models/04_bfm_emul_smem_ddr2_3/03_Src/emul_ifc1211_smem_ddr3.vhd
10 add_files -fileset simulation -norecurse modules/tosca2b/06_Simulation/02_Models/04_bfm_emul_smem_ddr2_3/03_Src/ddr3_4g.v
11
12 set_property include_dirs modules/xuser_example_0/06_Simulation/06_ModelSIM [current_fileset]
13
14 set_property top tstbench [get_filesets simulation]
15 set_property top_lib xil_defaultlib [get_filesets simulation]
16 update_compile_order -fileset simulation
17
```

Simulation script



Testbench & stimuli

top_tb.vhd - /home/rkielbik/work/Lodz_development/fw/sim/tb - Geany

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top_tb.vhd

```
491     for i in 0 to cb_pkg.NUM_OF_CHANNELS-1 loop
492
493       bank_selector := std_logic_vector(to_unsigned(i,16));
494
495       if i = 0 then
496         base_addr(i) := BASE_PAGE_ADDR_0 & x"000";
497       else
498         base_addr(i) := end_addr(i-1);
499       end if;
500
501       end_addr(i) := std_logic_vector(unsigned(base_addr(i)) + cb_pkg.BURST_MULTIPLIER * cb_pkg.BURST_BOUNDARY);
502       burst_size(i) := x"00000" & BURST_SIZE_256;
503       data_interrupt_threshold(i) := std_logic_vector((unsigned(end_addr(i)) - unsigned(base_addr(i))) / 2);
504       latency_threshold(i) := x"0000" & x"0004";        -- 4 ms
505       generator_parameters(i) := x"00" & x"000000";     -- rate: 0/0 - data generator disabled
506       sample_threshold(i) := x"0000" & x"01F0";
507
508       -- base_addr
509       reg_selector :=  std_logic_vector(to_unsigned(xuser_tcsr_pkg.REG_BASE_ADDR,16));
510       IO_WRITE_RQ   ("B_104_001", PCIE_0_BFM, cbrs_addr   , X"F", bank_selector & reg_selector);          wait for TIME_FOR_REGISTER_OPERATION;
511       IO_WRITE_RQ   ("B_104_001", PCIE_0_BFM, cbrv_addr   , X"F", base_addr(i));                         wait for TIME_FOR_REGISTER_OPERATION;
512
513       -- end_addr
514       reg_selector :=  std_logic_vector(to_unsigned(xuser_tcsr_pkg.REG_END_ADDR,16));
515       IO_WRITE_RQ   ("B_104_001", PCIE_0_BFM, cbrs_addr   , X"F", bank_selector & reg_selector);          wait for TIME_FOR_REGISTER_OPERATION;
516       IO_WRITE_RQ   ("B_104_001", PCIE_0_BFM, cbrv_addr   , X"F", end_addr(i));                           wait for TIME_FOR_REGISTER_OPERATION;
517
518       -- burst_size
519       reg_selector :=  std_logic_vector(to_unsigned(xuser_tcsr_pkg.REG_BURST_SIZE,16));
520       IO_WRITE_RQ   ("B_104_001", PCIE_0_BFM, cbrs_addr   , X"F", bank_selector & reg_selector);          wait for TIME_FOR_REGISTER_OPERATION;
521       IO_WRITE_RQ   ("B_104_001", PCIE_0_BFM, cbrv_addr   , X"F", burst_size(i));                         wait for TIME_FOR_REGISTER_OPERATION;
```

To do

1. Implement adding simulation sources in Makefile
2. Adapt stimuli to current configuration registers
3. Extend testbench (e.g. with models of new modules to be designed)