BPM electronics

(An overview of the requirements and the possible solutions for ESS)

EUROPEAN SPALLATION SOURCE

Hooman Hassanzadegan

ESS, Beam Instrumentation Group

EUROPEAN SPALLATION SOURCE

Outline

1. BPM system requirements
2. Platform for the BPM electronics
3. Overview of the signal detections methods for the BPM pickups
4. BPM electronics
   - Analog front end (RTM)
   - Digital unit
5. Timing requirements

EUROPEAN SPALLATION SOURCE

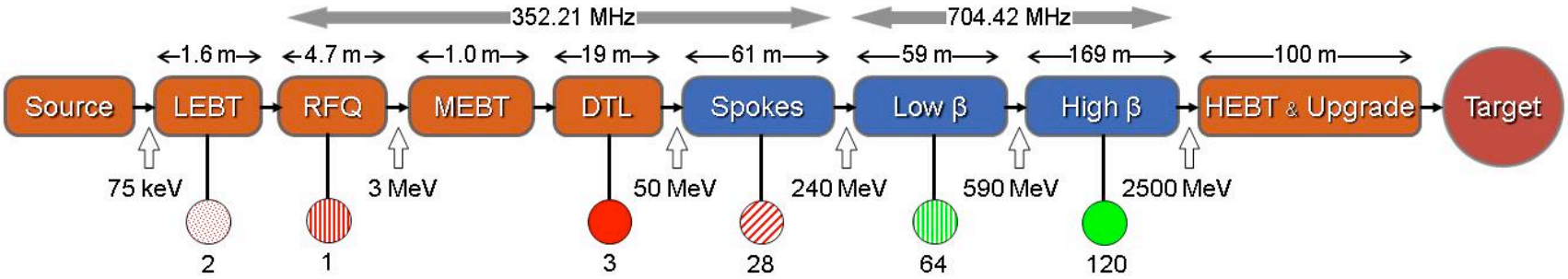
BPM system requirements

The total number of BPMs shall be 107 including:

- **MEBT:** 4
- **DTL:** 8 (2 per tank)
- **Spoke cavities:** 30
- **Low-β elliptical cavities:** 10
- **High-β elliptical cavities:** 28
- **HEBT:** 22

The BPM system shall be able to measure:

1. **Beam position**
2. **Beam phase**
3. **Beam intensity**

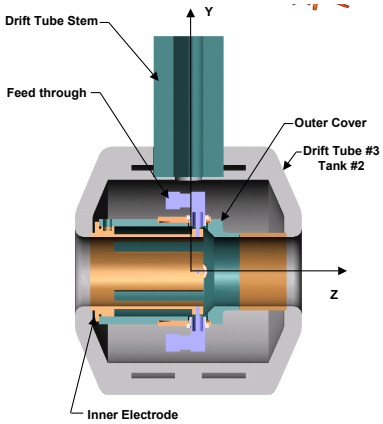


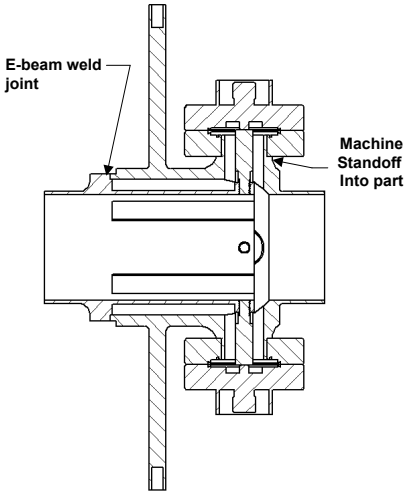
RF Power Sources (source output power and structure input power)

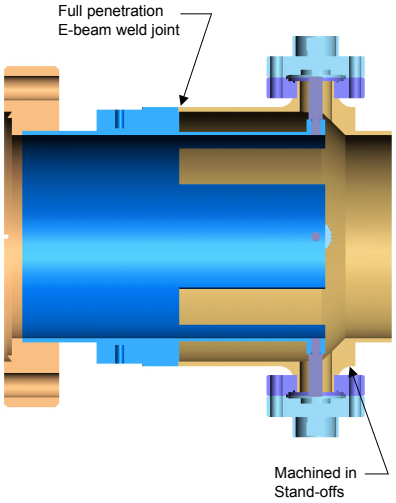
- 2800 kW (2000 kW) 352.21 MHz
- 1200 kW (900 kW) 352.21 MHz
- 400 kW (300 kW) 352.21 MHz
- 1500 kW (900 kW) 704.42 MHz
- 700 kW (500 kW) 704.42 MHz
- 30 kW (16 kW) 352.21 MHz

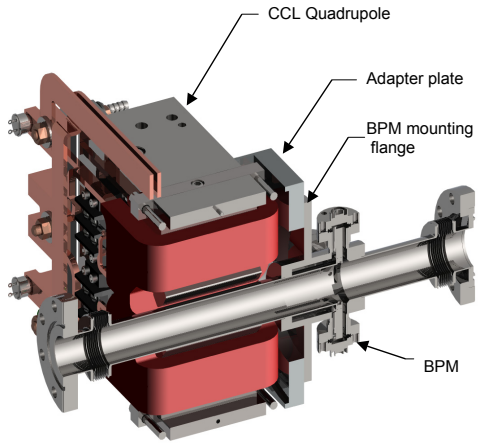
BPM system requirements (cont'd)

The BPM pickups will have different designs. Nevertheless, it is planned to use the same type of electronics for all the pickups.



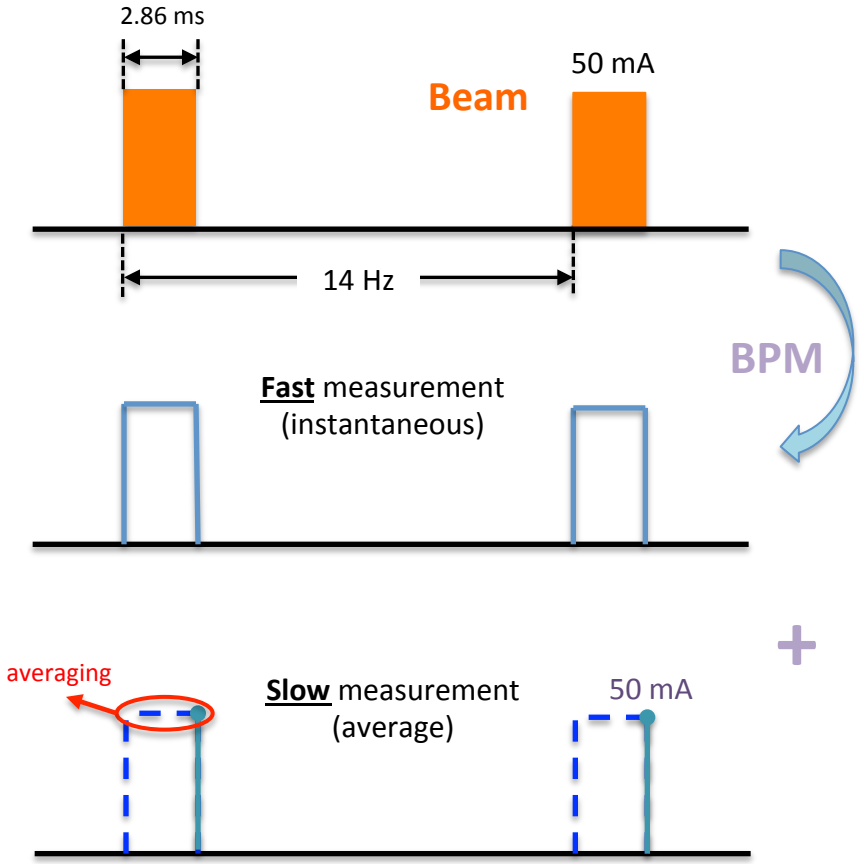


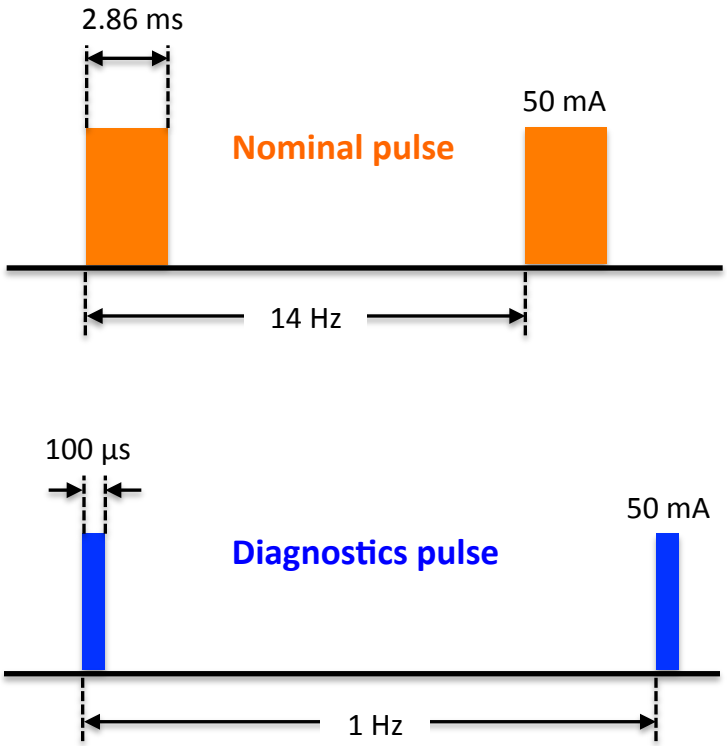




Pickup pictures from SNS, Jim O'Hara, LNAL, "SNS Linac Beam Position Monitor pickups", 2002

BPM system requirements (cont'd)



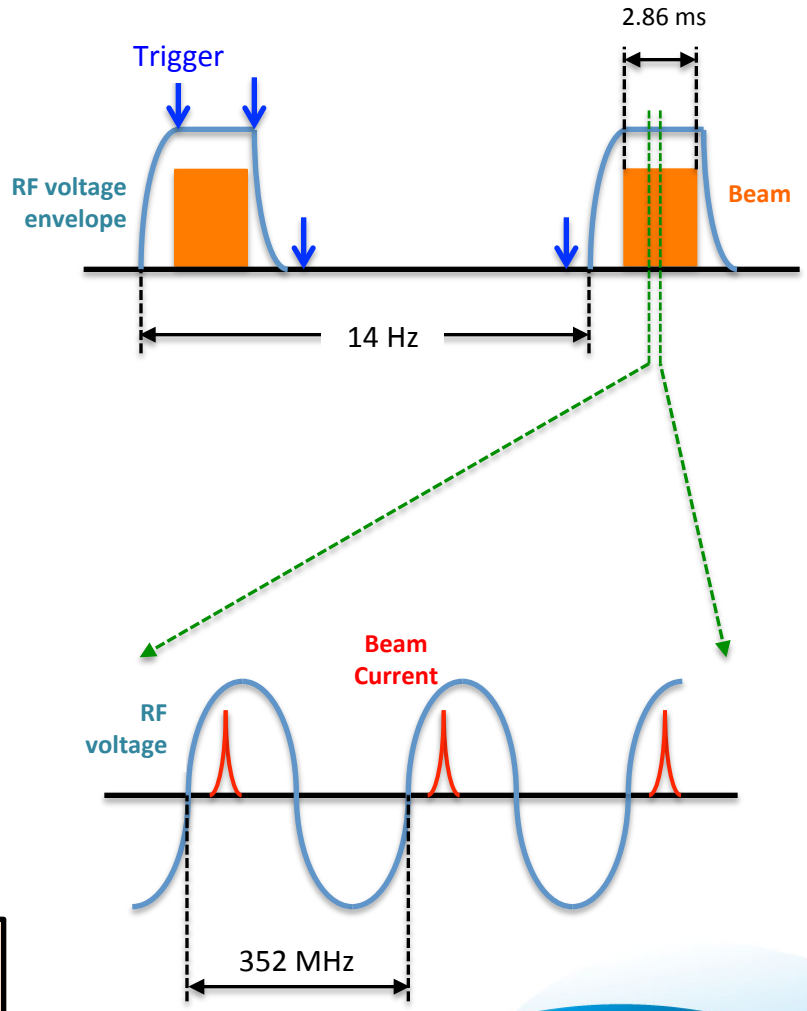


The BPM system shall be able to make a fast and a slow measurement of the beam position, phase and intensity in nominal and diagnostics pulse modes.

EUROPEAN SPALLATION SOURCE

BPM system requirements (cont'd)

➢ **Beam position accuracy:**	**±100 µm (RMS)**
➢ **Beam position resolution:**	**20 µm**
➢ **Phase measurement accuracy:**	**±1° (RMS)**
➢ **Phase measurement resolution:**	**0.2°**
➢ **Measurement range:**	**50% of the beam pipe dia.**
➢ **Phase measurement range:**	**±180°**
➢ **ADC sample rate:**	**> 1 MSPS**
➢ **Electronics response time:**	**< 1 µs**
➢ **Refresh rate (end user):**	**14 Hz**



We are discussing with the Beam Physics group to finalize the requirements.

EUROPEAN SPALLATION SOURCE

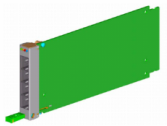
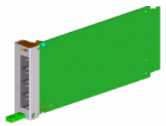
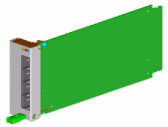
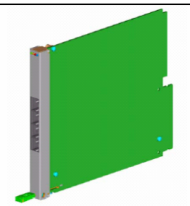
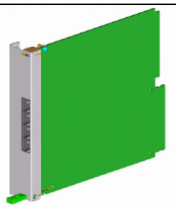
Electronics platform comparison

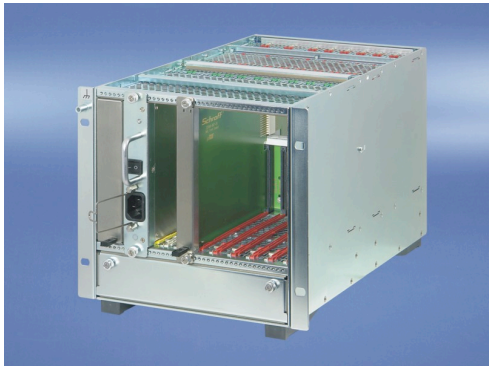
	VXS	µTCA	PXI	cPCI/cPCIe
Vendor number	16+	~10	70+	Many
Maturity	Medium	Medium	High	High
Max. transfer rate	Star/dual star: 30Gbps, Mesh: 112 Gbps	1 GbE, 2GbE, 10 GbE; Up to 12.5 Gbps 250MB/s/lane (PCIe)	PXI: 132 MB/s PXIe: 250 MB/s/lane (up to 16 lanes)	PCI: 132 MB/s PCIe: 250 MB/s/lane (up to 16 lanes)
Backplane timing and synchronization	112 S.E. pins, 32 diff. pairs	84 pair for MCH, 7 pairs per AMC for 12 AMCs	10 MHz and 100 MHz clock, 8x shared trigger, star triggers	
Topology	Star, dual star, full mesh	Star, dual star, full mesh	Master-slave, star	Master-slave, star
Redundancy	YES	YES	Power Supply only	Power Supply only
Users	Military, Avionics	DESY XFEL	EBG MedAustron,…	CERN, LANL, ORNL, ITER (planned), JET, ETE, EBG MedAustron
Crate cost	High (From 3000 €)	Medium (From 2000 €)	Medium (From 880 € for 4 slot version)	Medium (From 900 € for 6 slot version)
Documentation		Poor	Fair	Good
Ease of use		Fair	Easy to start	Fair
RTM	NO	YES	NO (alternative: FlexRIO)	NO
Power	90 W (5V), 66W (3.3V)	20 – 80 W per slot	30 W per slot	30 W per slot

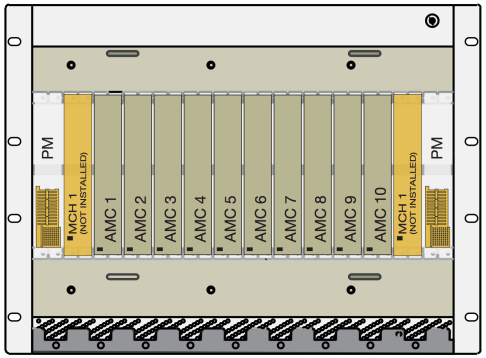
Full table by Miha Rescic from Cosylab (Currently working at ESS)

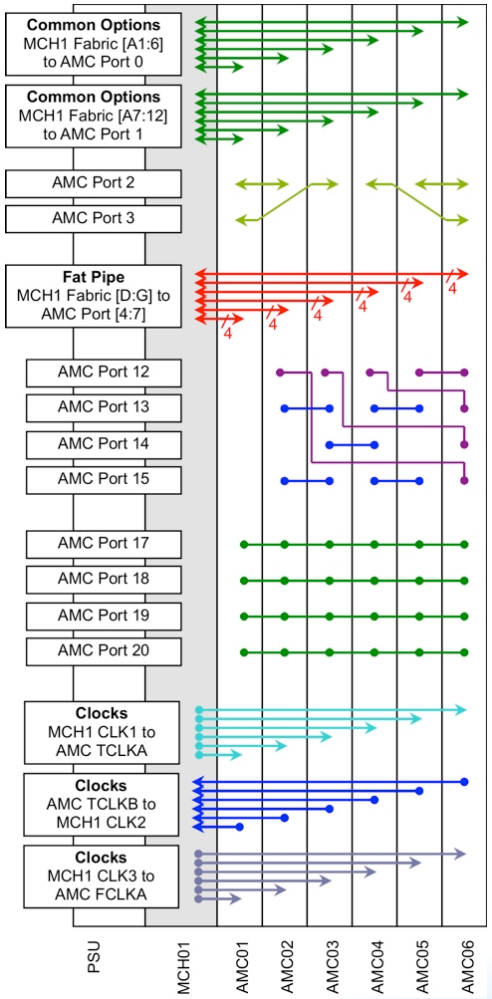
EUROPEAN SPALLATION SOURCE

µTCA chassis platform

	Compact-Size (3HP)	Mid-Size (4HP)	Full-Size (6HP)
Single modules	 73.8x13.88x181.5mm	 73.8x18.96x181.5mm	 73.8x28.95x181.5mm
Double modules	 148.8x13.88x181.5mm	 148. 8x18.96x181.5mm	 148. 8x28.95x181.5mm

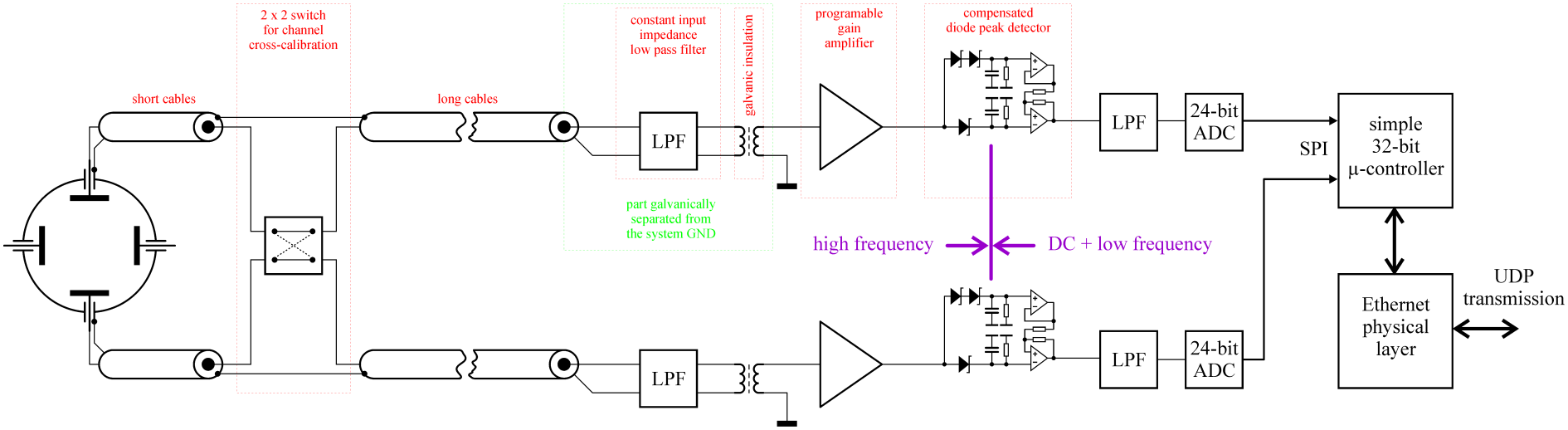






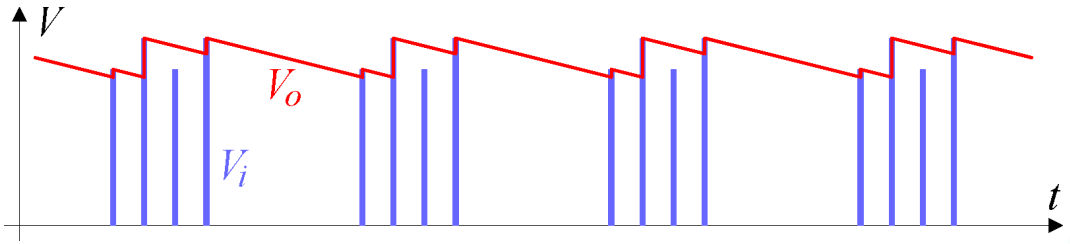
BPM signal detection – method 1

Simple diode detector and S&H + LPF (LHC – CERN and DESY)



Diode Orbit Measurement

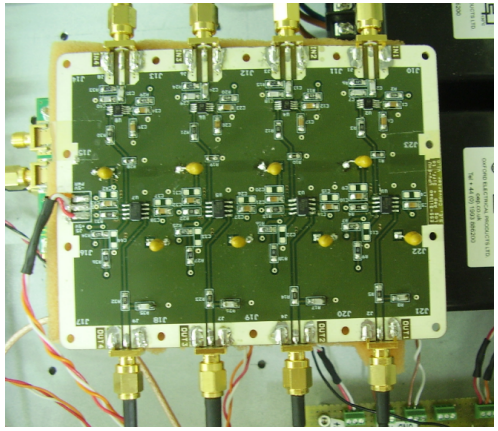
2 channels shown for one pick-up plane,
one 19" 1U unit accommodates 8 channels



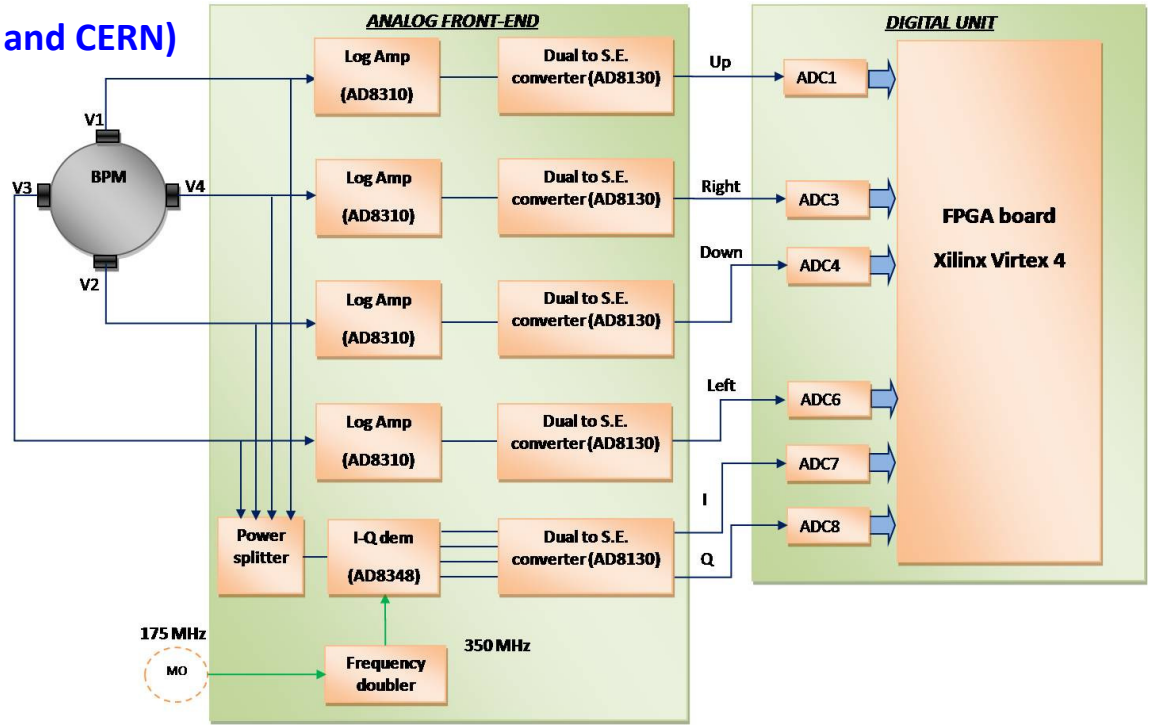
From Marek Gasior's presentation at the DITANET workshop at CERN, Jan 2012

BPM signal detection – method 2

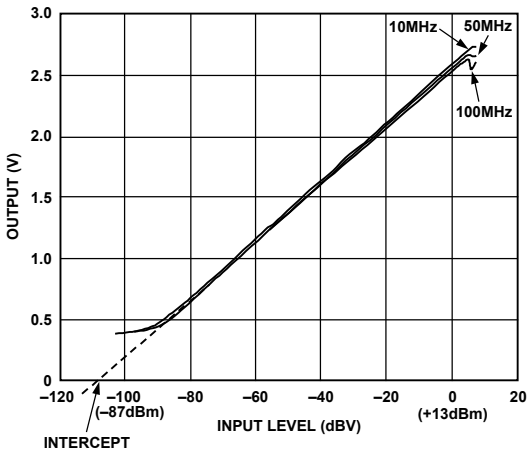
Signal detection with log-amps (ESS-B and CERN)



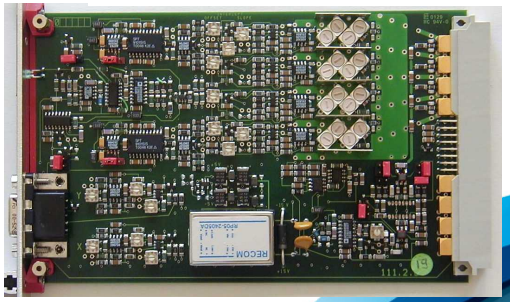
ESS-Bilbao log-amp detector board



ESS-Bilbao BPM system



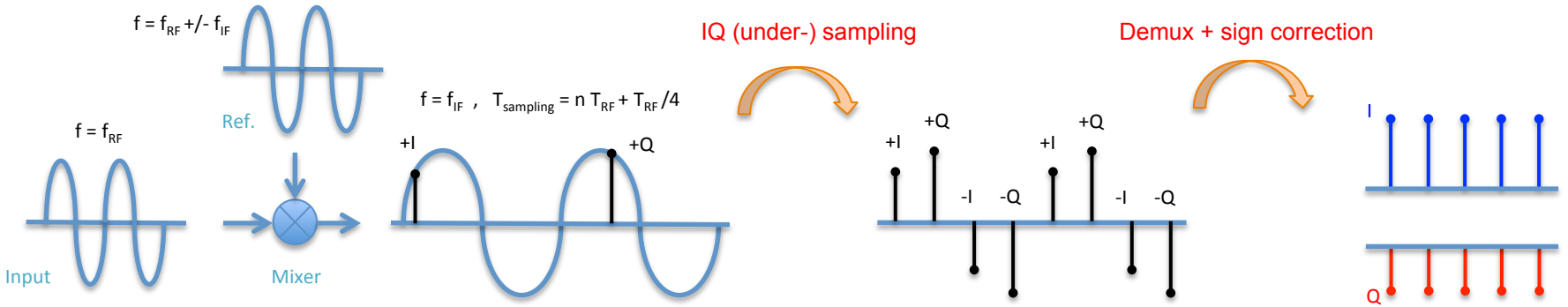
AD8310 response



Commercial log-amp detector

BPM signal detection – method 3

Down-conversion to IF + IQ sampling (SNS)



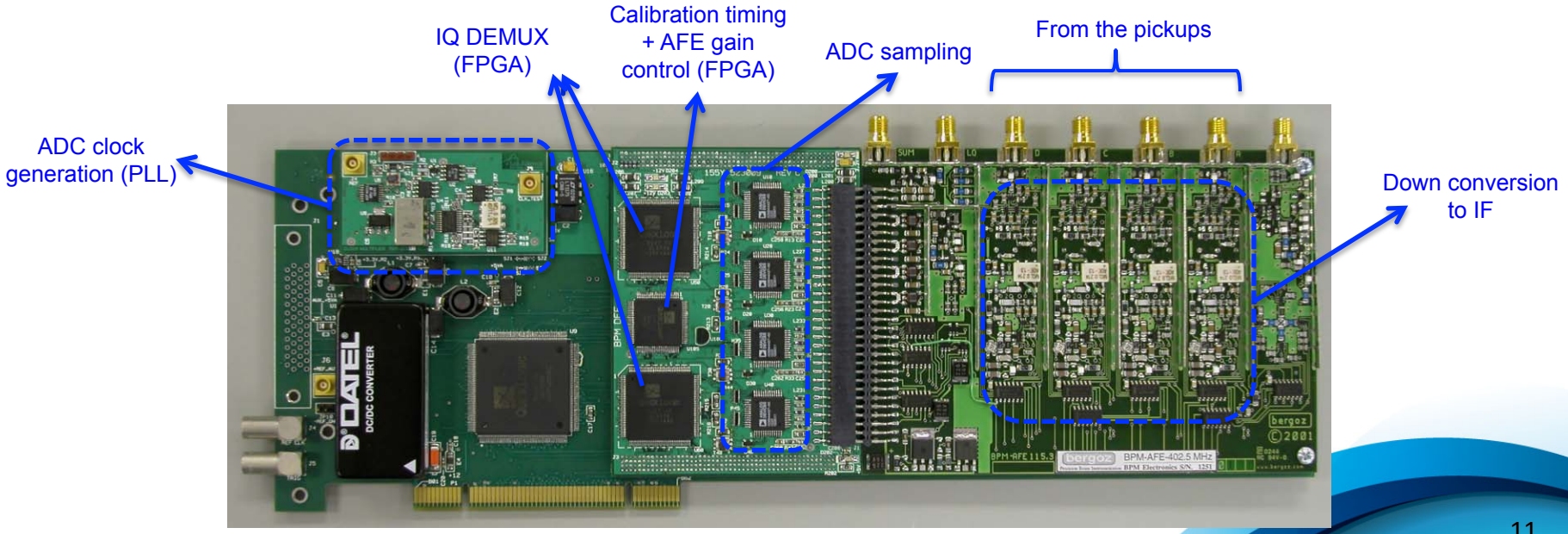
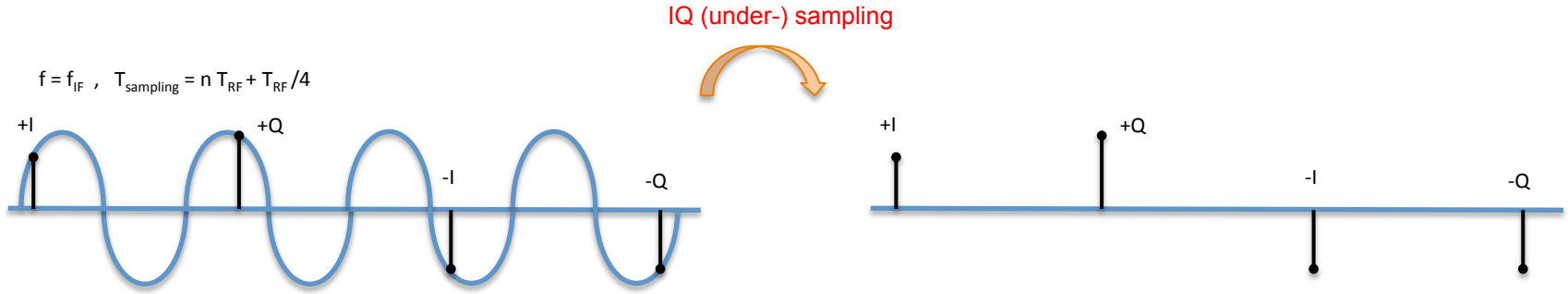


Photo ref: J. Power et al. , Beam Position Monitor System for the SNS LINAC, Proc. PAC 2003

BPM signal detection – method 4

Direct IQ sampling (or under-sampling) in RF:

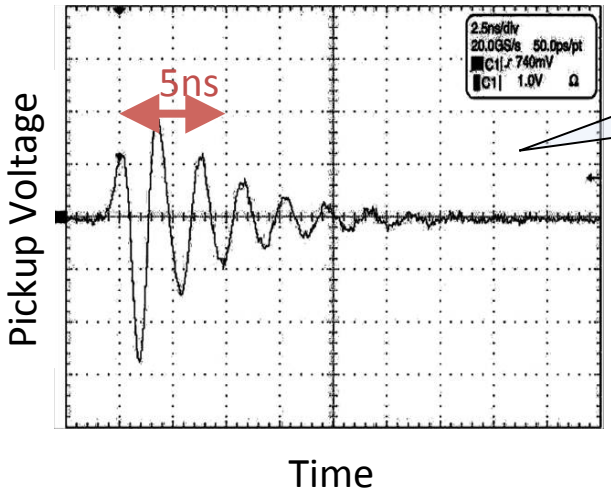


352 MHz (or 704 MHz) signal from the detector (after filtering)

Direct sampling in RF would simplify the AFE due to the elimination of the RF-IF stage, but there could be issues with the zone-3 connector which might not be suitable for transferring a high frequency signal.

BPM signal detection - method 5

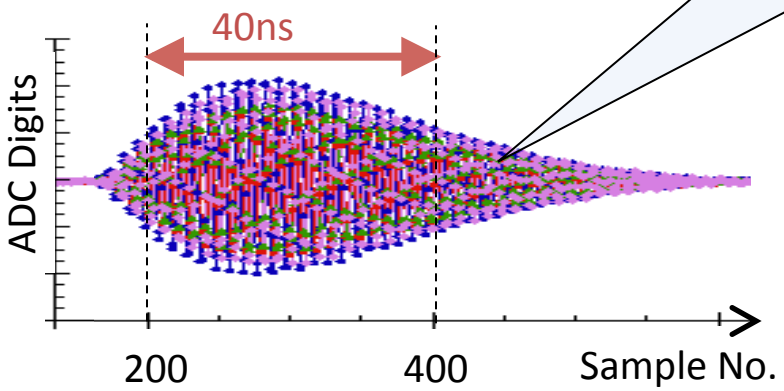
Ringing filter + ADC sampling at very high frequency (SLS):

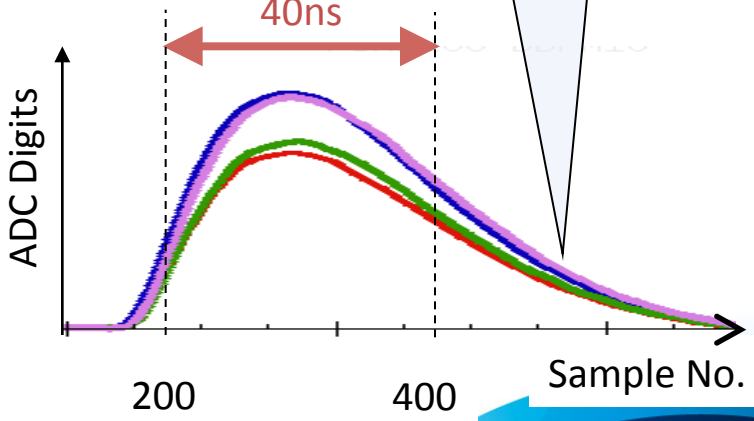


Low-passed pickup signal (scope measurement).

RFFE output, digitized by BPM electronics (5Gsps), after gain/offset/jitter correction & FIR filtering in FPGA.

FPGA calculates envelopes of RFFE signals. Beam position calculated from integrals.





Slide from Boris Keil's presentation at the DITANET workshop at CERN, Jan 2012

EUROPEAN SPALLATION SOURCE

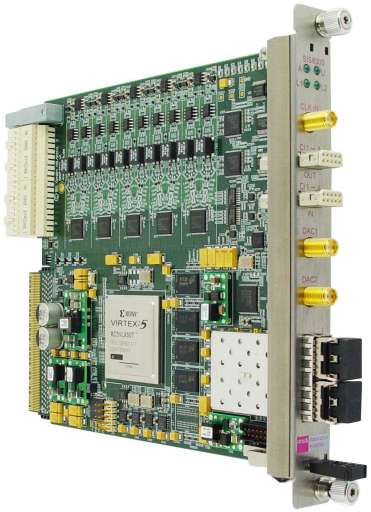
Comparison of signal detection methods

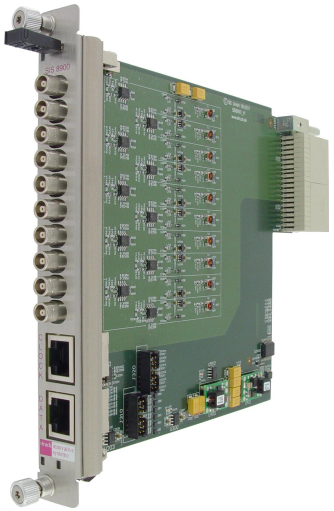
	Diode	Log. Amp.	Down mixing + sampling in IF	Sampling in RF	Ringing filter + Fast ADC
Complexity	Low	Low	Medium-high	Medium	high
Cost	Low	Low	High	Medium-High	Very high
Performance	Acceptable	Fair	Good	Good	Good
Possibility of use for LLRF	No	No	Yes	Yes	No

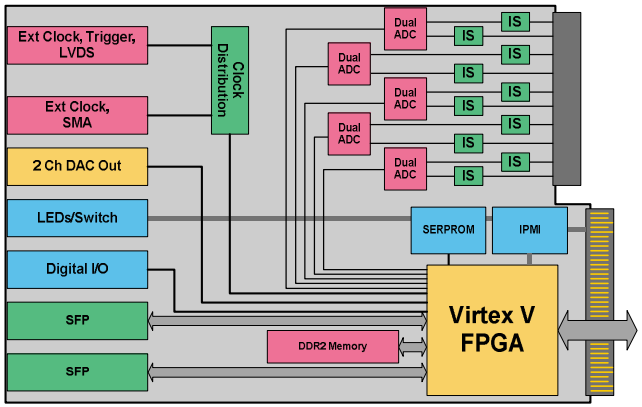
Not Compatible with LLRF

Compatible with LLRF

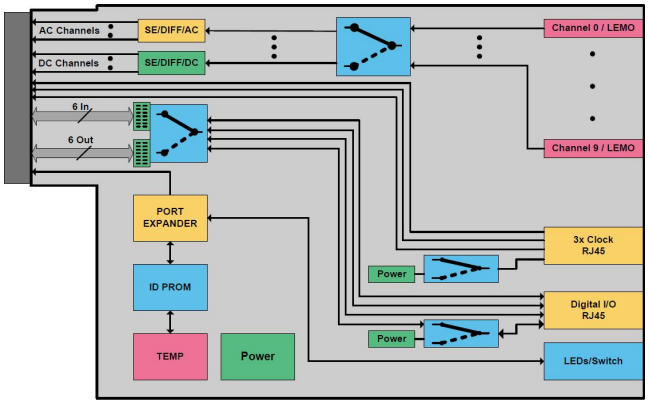
BPM electronics (analog + digital)







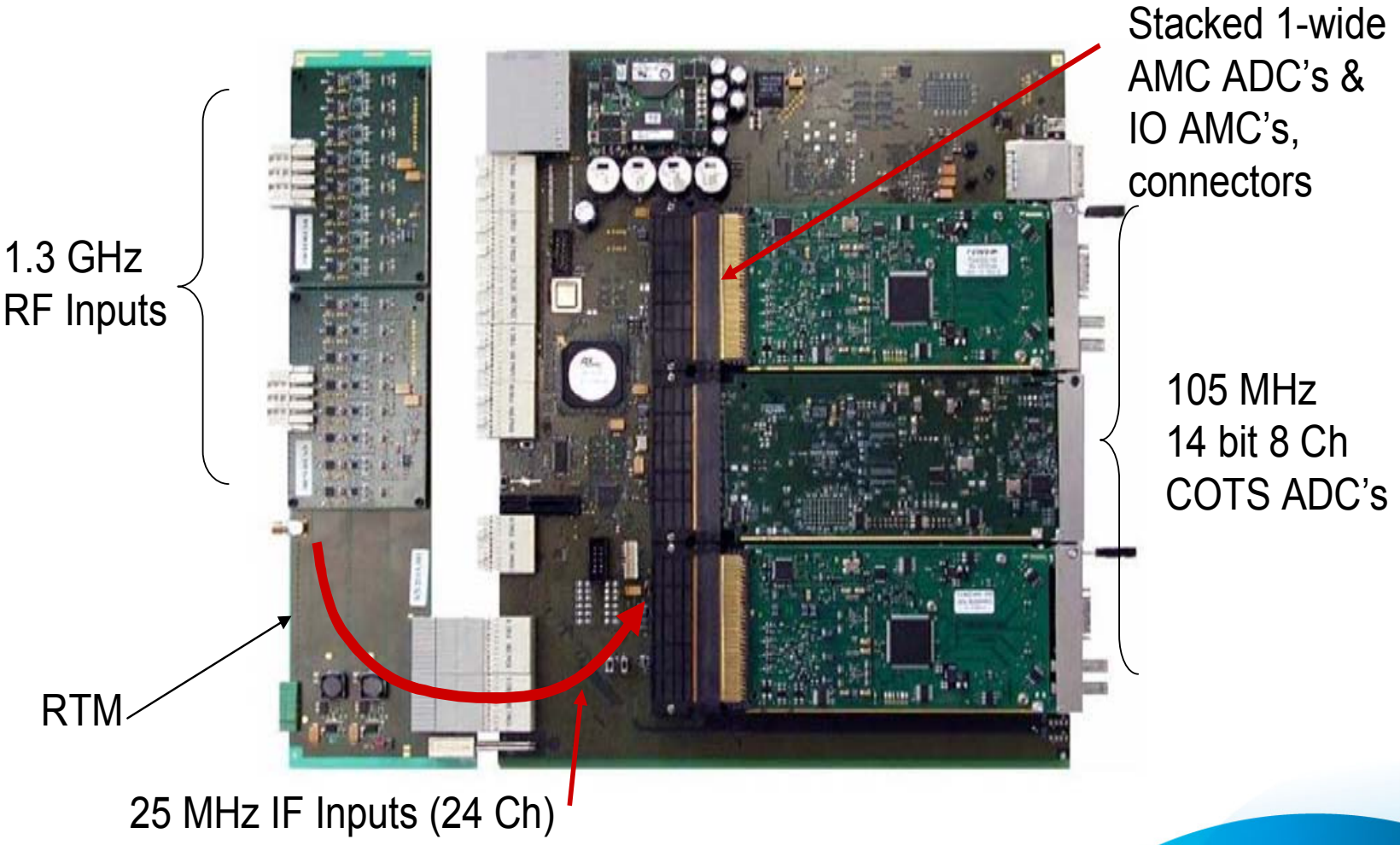
Commercial MTCA.4 module (10 ADCs + 2 DACs + Virtex-5 FPGA



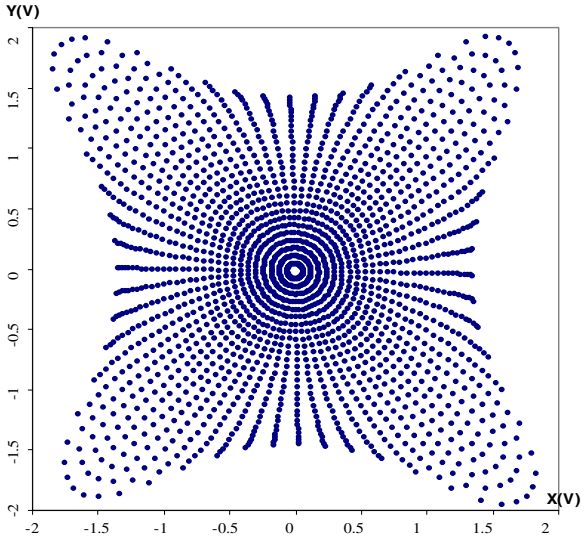
Commercial micro-RTM

EUROPEAN SPALLATION SOURCE

ATCA-based LLRF electronics (DESY)



Auto-calibration and linearization



Maurice Cohen-Solal, Design, test and calibration of an electrostatic beam position monitor, Ph. Rev. ST - AB

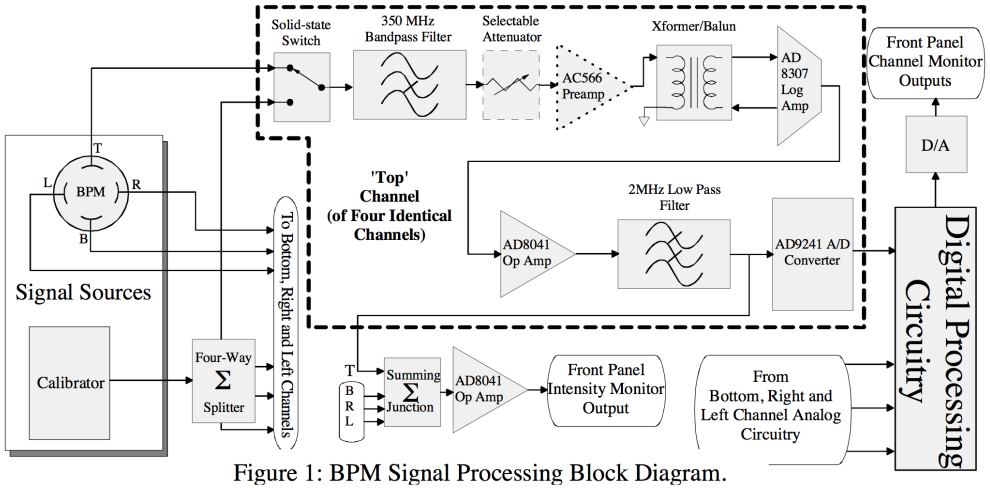
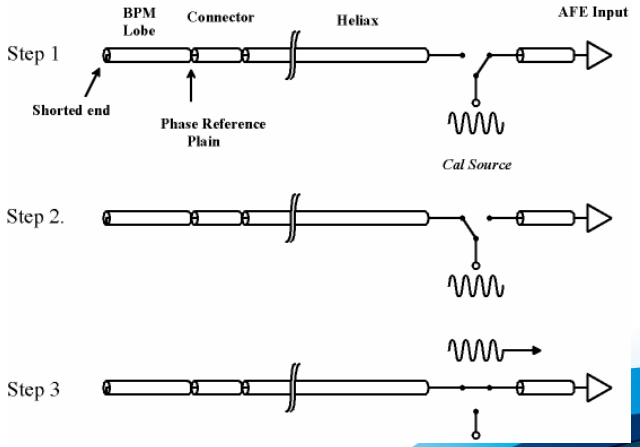


Figure 1: BPM Signal Processing Block Diagram.

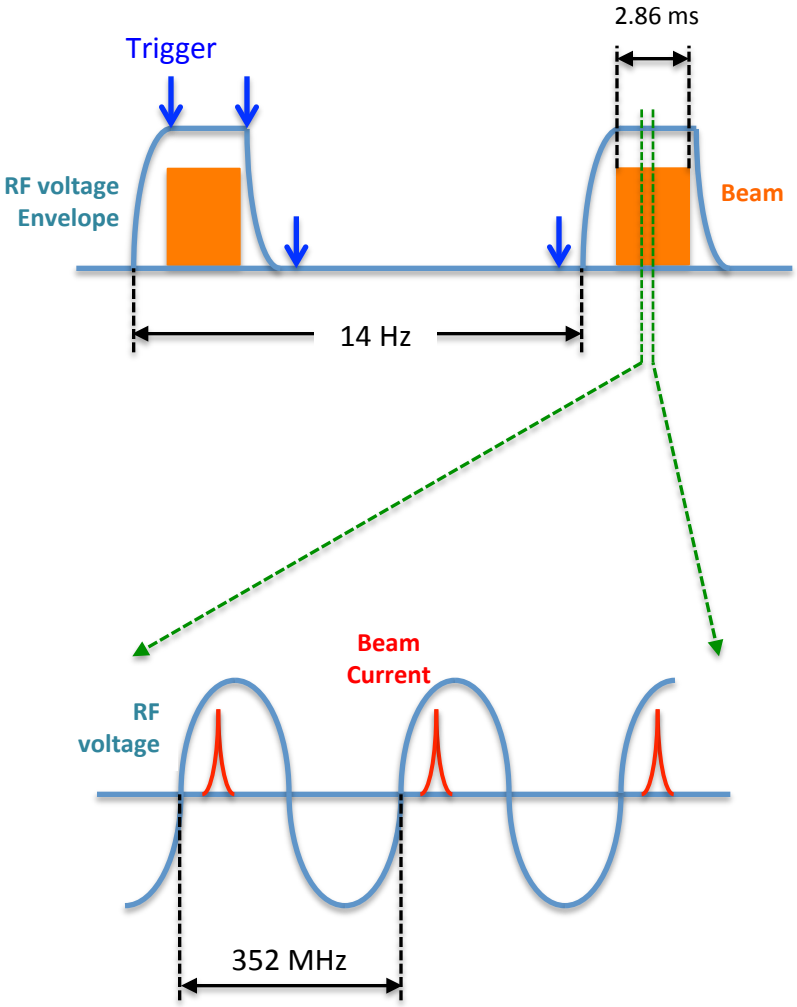
R. B. Shurter et. Al, Analog Front-end Electronics for Beam Position Measurement on the Beam Halo Measurement, Proc. PAC'01

DC offset compensation, linearization and auto-calibration shall be done by the FPGA.



J. Power et al, "Beam Position Monitor Systems for the SNS Linac", PAC'03

Timing requirements for the BPM system



Intra-pulse:

- ADC sampling
- Data storage on the AMC memory, etc.

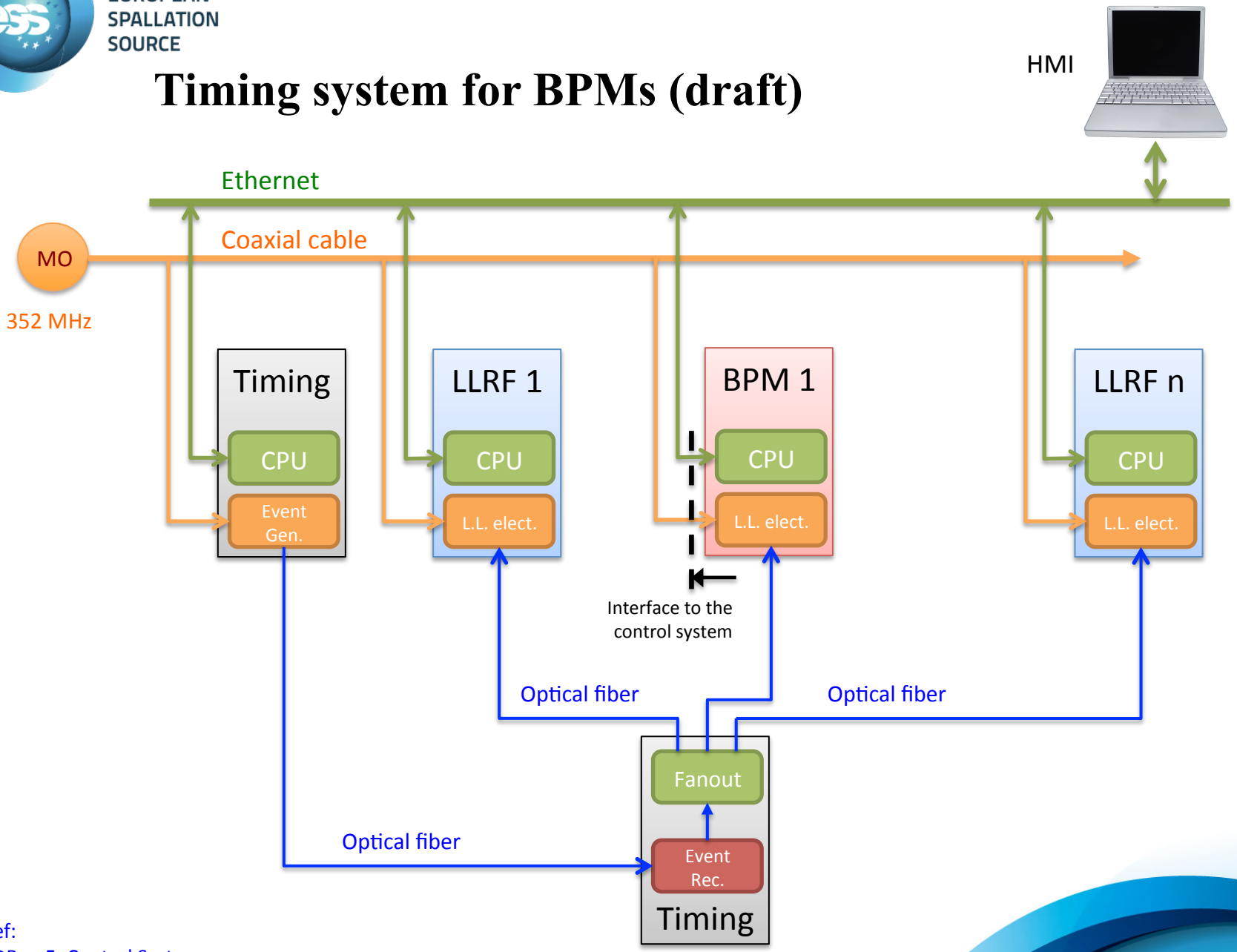
Inter-pulse:

- Data communication to the control system
- Auto calibration
- Error compensation, etc.

RF reference phase:

- RF phase detection
- IQ demodulation

Timing system for BPMs (draft)



Ref:
CDR -> 5. Control Systems
CDR -> 4.8.2 Low Level RF control

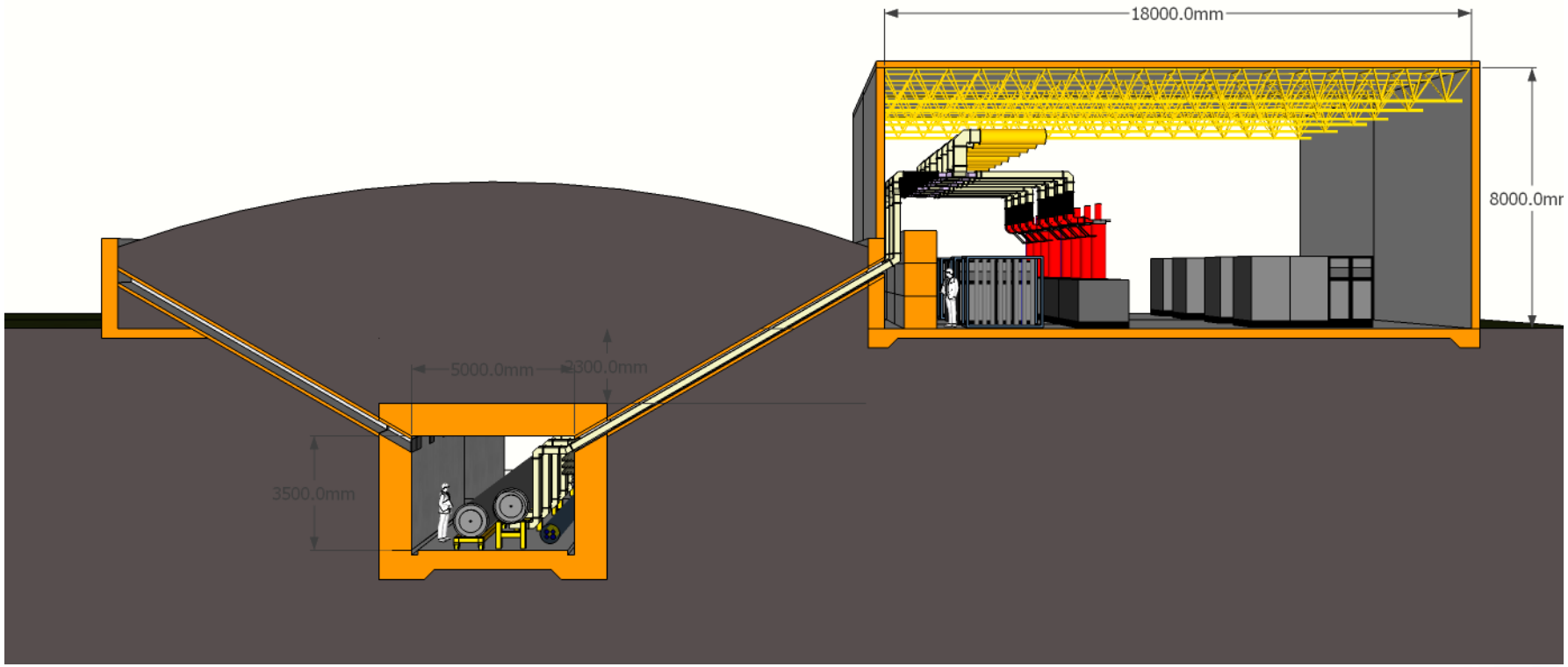
EUROPEAN SPALLATION SOURCE

Summary of the minimum timing requirements for the LLRF and BPM systems

Timing signal	Freq.	Synchronization	Spec.	Source	Comment
RF ref. ph.	352 MHz or 704 MHz	Synchronization needed for the whole Linac	Drift: <0.5°	Coaxial cable or Optical fiber	
Pulse rate	14 Hz	Synchronization needed for the whole Linac	Stability: 1ppm	Event based	+ Programmable delay
ADC/DAC sampling	10 MHz – 100 MHz	Synchronization needed within the shelf		backplane	shelf-to-shelf synchronization might also be needed for relative phase measurements
Non real-time or slow	---	Not needed	---	Ethernet	
Calibration ref. (BPM)	352 MHz or 704 MHz	Not needed		Internal to the shelf	

EUROPEAN SPALLATION SOURCE

Space allocation for the electronics



RF distribution from the klystron gallery to the tunnel, source: ESS RF group