

Timing Distribution - NCL

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2020-01-30

- Installation
- Deployment
- Validation
- Supercycle
- Workflow
- Conclusions

Installation

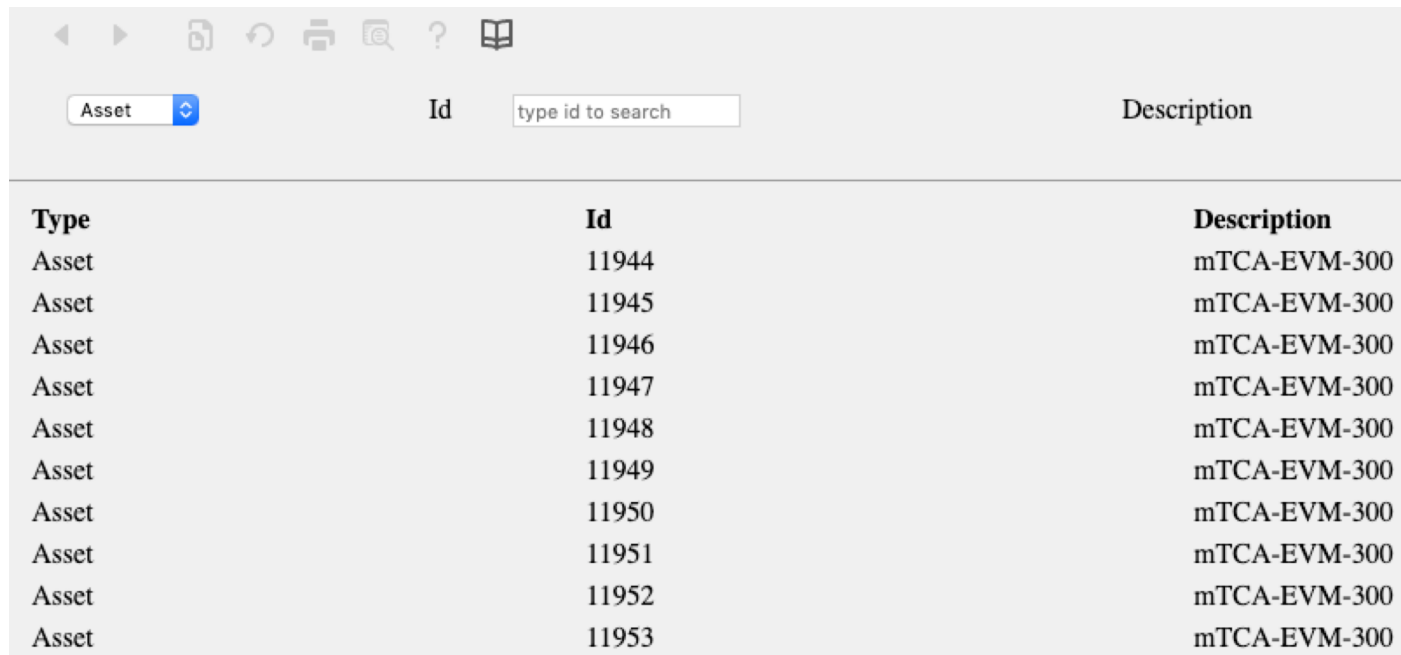
- Timing Distribution (TD) Eplan Drawings
 - NCL: mid 202002
- FBS
 - Status: released
- ESS/Epics names
 - Status: released
- TD-M (Master)
 - EAM asset codes
 - Status: subscribed for each card.
 - Installation
 - Status: mid 202002 in MBL-070ROW:CNPW-U-017
 - RF Front End Integration Tests: SAT and SIT
- TD-D2X where X belongs to NCL: ESS-1404467
 - March, April, May 2020

Installation – FBS (Chess)

	<input type="checkbox"/>		Tag 	Description 
1.	<input type="checkbox"/>	 K01	=ESS.INFR.K01	Timing Distribution System
2.	<input type="checkbox"/>	 K01	=ESS.INFR.K01.K01	TM/TD0 Event Master
3.	<input type="checkbox"/>	 K02	=ESS.INFR.K01.K02	TD1-1 Timing System Controller
4.	<input type="checkbox"/>	 K03	=ESS.INFR.K01.K03	TD1-2 Timing System Controller
5.	<input type="checkbox"/>	 K04	=ESS.INFR.K01.K04	TD2-1 Timing System Controller
6.	<input type="checkbox"/>	 K05	=ESS.INFR.K01.K05	TD2-2 Timing System Controller
7.	<input type="checkbox"/>	 K06	=ESS.INFR.K01.K06	TD2-3 Timing System Controller
8.	<input type="checkbox"/>	 K07	=ESS.INFR.K01.K07	TD2-4 Timing System Controller
9.	<input type="checkbox"/>	 K08	=ESS.INFR.K01.K08	TD2-5 Timing System Controller
10.	<input type="checkbox"/>	 K09	=ESS.INFR.K01.K09	TD2-6 Timing System Controller
11.	<input type="checkbox"/>	 K10	=ESS.INFR.K01.K10	TD2-7 Timing System Controller
12.	<input type="checkbox"/>	 K11	=ESS.INFR.K01.K11	TD2-8 Timing System Controller
13.	<input type="checkbox"/>	 K12	=ESS.INFR.K01.K12	TD2-9 Timing System Controller
14.	<input type="checkbox"/>	 K13	=ESS.INFR.K01.K13	TD2-10 Timing System Controller
15.	<input type="checkbox"/>	 K14	=ESS.INFR.K01.K14	TD2-11 Timing System Controller
16.	<input type="checkbox"/>	 K15	=ESS.INFR.K01.K15	TD2-12 Timing System Controller
17.	<input type="checkbox"/>	 K16	=ESS.INFR.K01.K16	TD2-13 Timing System Controller
18.	<input type="checkbox"/>	 K17	=ESS.INFR.K01.K17	TD2-14 Timing System Controller
19.	<input type="checkbox"/>	 K18	=ESS.INFR.K01.K18	TD2-15 Timing System Controller
20.	<input type="checkbox"/>	 K19	=ESS.INFR.K01.K19	TD2-16 Timing System Controller
21.	<input type="checkbox"/>	 K20	=ESS.INFR.K01.K20	TD2-17 Timing System Controller
22.	<input type="checkbox"/>	 K21	=ESS.INFR.K01.K21	TD2-18 Timing System Controller
23.	<input type="checkbox"/>	 K22	=ESS.INFR.K01.K22	TD2-19 Timing System Controller
24.	<input type="checkbox"/>	 K23	=ESS.INFR.K01.K23	TD2-20 Timing System Controller
25.	<input type="checkbox"/>	 K24	=ESS.INFR.K01.K24	TD2-21 Timing System Controller
26.	<input type="checkbox"/>	 K25	=ESS.INFR.K01.K25	TD2-22 Timing System Controller
27.	<input type="checkbox"/>	 K26	=ESS.INFR.K01.K26	TD2-23 Timing System Controller
28.	<input type="checkbox"/>	 K27	=ESS.INFR.K01.K27	TD2-24 Timing System Controller
29.	<input type="checkbox"/>	 K28	=ESS.INFR.K01.K28	TD2-25 Timing System Controller
30.	<input type="checkbox"/>	 K29	=ESS.INFR.K01.K29	TD2-26 Timing System Controller
31.	<input type="checkbox"/>	 K30	=ESS.INFR.K01.K30	TD2-27 Timing System Controller
32.	<input type="checkbox"/>	 K31	=ESS.INFR.K01.K31	TD2-28 Timing System Controller
33.	<input type="checkbox"/>	 K32	=ESS.INFR.K01.K32	TD2-29 Timing System Controller
34.	<input type="checkbox"/>	 K33	=ESS.INFR.K01.K33	TD2-30 Timing System Controller

Installation – Epics Names

Device Group ↕	Device Type ↕	Device Name ↕	Description ↕
Infrastructure	CPU	TD-D11:TS-CPU-01 ↗	CPU
Infrastructure	EVM	TD-D11:TS-EVM-01 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D11:TS-EVM-02 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D11:TS-EVM-03 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D11:TS-EVM-04 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D11:TS-EVM-05 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D11:TS-EVM-06 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D11:TS-EVM-07 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D11:TS-EVM-08 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D11:TS-EVM-09 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D11:TS-EVM-10 ↗	EVM Fanout/Concentrator
Infrastructure	MCH	TD-D11:TS-MCH-01 ↗	MTCA hub
Infrastructure	MTCA	TD-D11:TS-MTCA-01 ↗	MTCA crate
Infrastructure	PS	TD-D11:TS-PS-01 ↗	Wiener PM A1000
Infrastructure	PS	TD-D11:TS-PS-02 ↗	Wiener PM A1000
Infrastructure	CPU	TD-D12:TS-CPU-01 ↗	CPU
Infrastructure	EVM	TD-D12:TS-EVM-01 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D12:TS-EVM-02 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D12:TS-EVM-03 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D12:TS-EVM-04 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D12:TS-EVM-05 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D12:TS-EVM-06 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D12:TS-EVM-07 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D12:TS-EVM-08 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D12:TS-EVM-09 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D12:TS-EVM-10 ↗	EVM Fanout/Concentrator
Infrastructure	MCH	TD-D12:TS-MCH-01 ↗	MTCA hub
Infrastructure	MTCA	TD-D12:TS-MTCA-01 ↗	MTCA crate
Infrastructure	PS	TD-D12:TS-PS-01 ↗	Wiener PM A1000
Infrastructure	PS	TD-D12:TS-PS-02 ↗	Wiener PM A1000
Infrastructure	CPU	TD-D21:TS-CPU-01 ↗	CPU
Infrastructure	EVM	TD-D21:TS-EVM-01 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D21:TS-EVM-02 ↗	EVM Fanout/Concentrator
Infrastructure	EVM	TD-D21:TS-EVM-03 ↗	EVM Fanout/Concentrator
Infrastructure	MCH	TD-D21:TS-MCH-01 ↗	MTCA hub
Infrastructure	MTCA	TD-D21:TS-MTCA-01 ↗	MTCA crate
Infrastructure	PS	TD-D21:TS-PS-01 ↗	Wiener PM A1000



The screenshot shows a web application interface with a toolbar at the top containing navigation icons (back, forward, home, refresh, print, search, help, and a book icon). Below the toolbar is a search bar with a dropdown menu set to 'Asset', a label 'Id', and a text input field containing 'type id to search'. The main content area displays a table with three columns: 'Type', 'Id', and 'Description'. The table contains ten rows of data, all with 'Asset' in the 'Type' column and 'mTCA-EVM-300' in the 'Description' column. The 'Id' values range from 11944 to 11953.

Type	Id	Description
Asset	11944	mTCA-EVM-300
Asset	11945	mTCA-EVM-300
Asset	11946	mTCA-EVM-300
Asset	11947	mTCA-EVM-300
Asset	11948	mTCA-EVM-300
Asset	11949	mTCA-EVM-300
Asset	11950	mTCA-EVM-300
Asset	11951	mTCA-EVM-300
Asset	11952	mTCA-EVM-300
Asset	11953	mTCA-EVM-300

Deployment

TD-M

```
# Maintenance
epicsEnvSet("LOCATION","MBL-070ROW:CNPW-U-017") # Location
epicsEnvSet("FBS","=ESS.INFR.K01.K01")      # The parent node of AS

# Naming: AS:DS-ID
epicsEnvSet("AS",      "TD-M")              # Area Structure
# SCE IOC
epicsEnvSet("DSSCE",  "TS-SCE")            # Device Structure SCE
epicsEnvSet("PSCE01", "$(AS):$(DSSCE)-01:") # Prefix of the SCE 01
# EVG IOC
epicsEnvSet("DSEVG",  "TS-EVG")            # Device Structure EVG
epicsEnvSet("PEVG01", "$(AS):$(DSEVG)-01:") # Prefix of the EVG 01
```

NFS Mount



icshwi / e3-mrfioc2

<> Code ! Issues 0 Pull requests 1 Actions

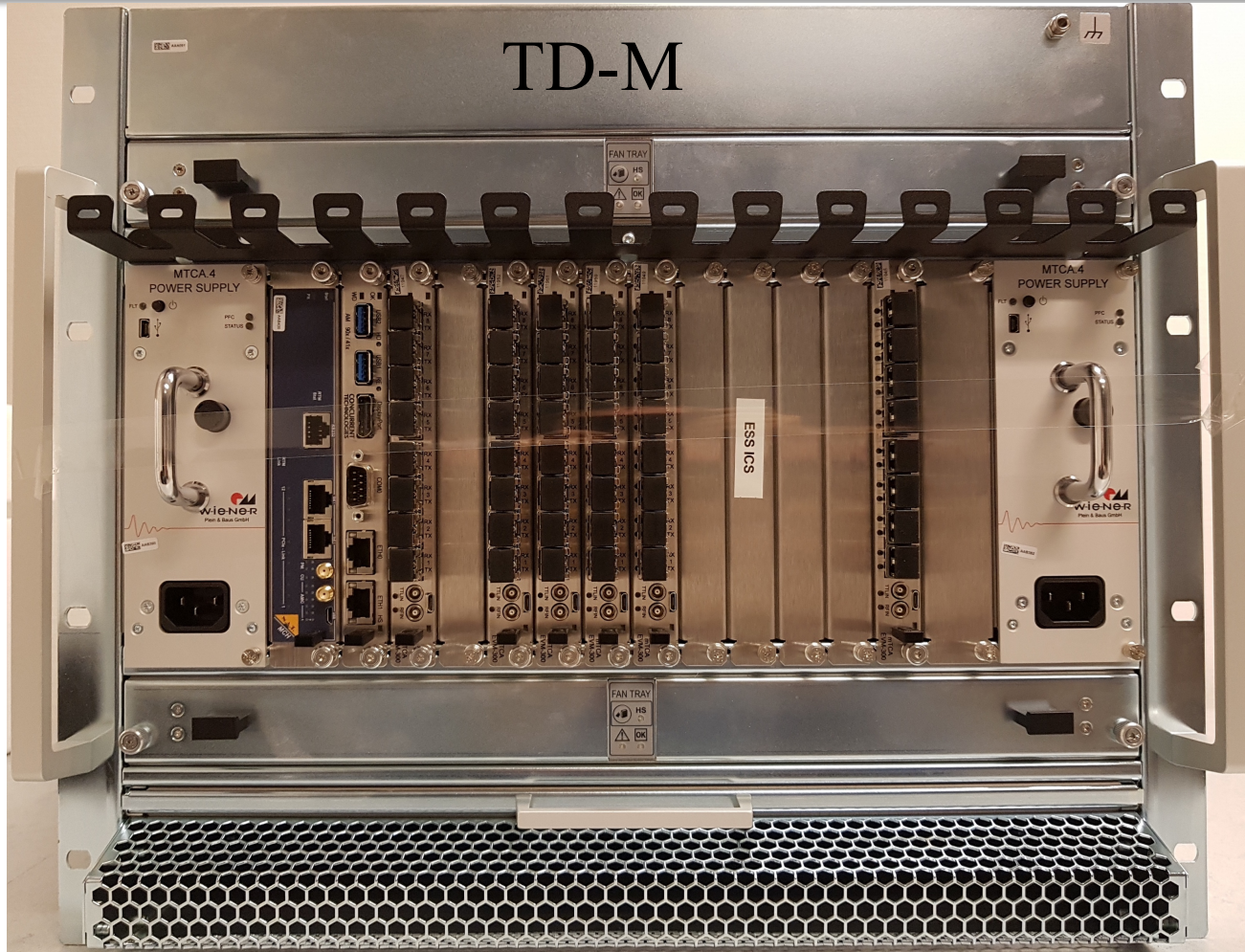
ESS Site-specific EPICS module : mrfioc2

ess-epics-environment Manage topics

285 commits 7 branches

Under revision

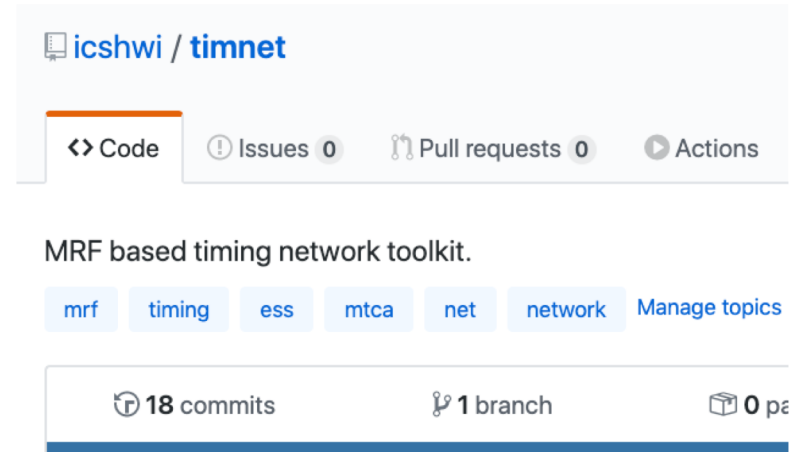
Deployment - Hardware



Ready

Validation

- “timnet” App (Alpha Release)
 - To expose the timing network topology, parameters and states
 - Background for an eventual timing network GUI development
 - Maintenance checks after changes or shutdowns
 - SAT and SIT purposes
 - Timing network monitoring



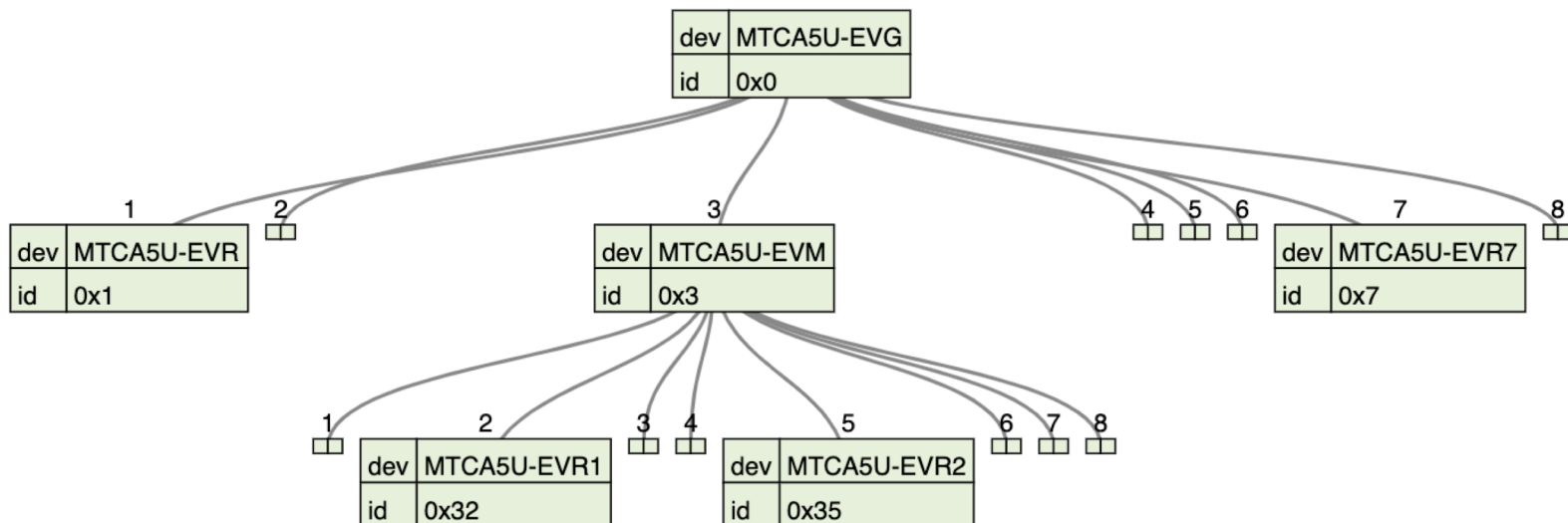
icshwi / timnet

<> Code Issues 0 Pull requests 0 Actions

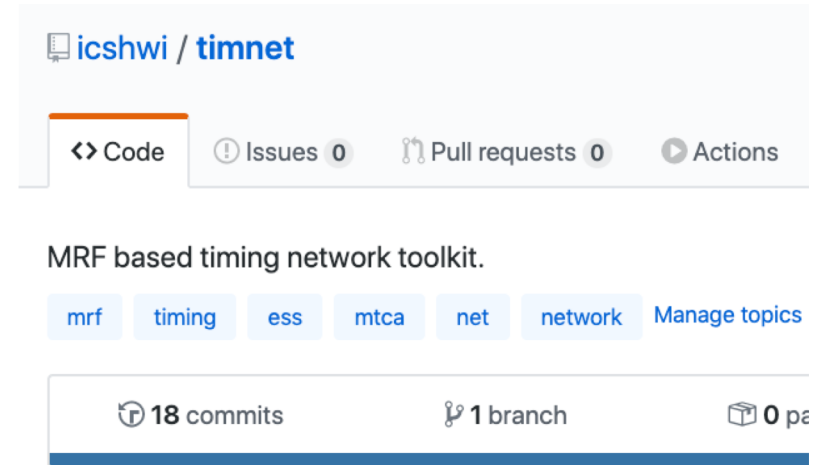
MRF based timing network toolkit.

mrf timing ess mtca net network Manage topics

18 commits 1 branch 0 packages



- “timtest” App (Not Finished)
 - Stress tests – One week.
 - Firmware
 - Image
 - Status: backlog
- State definition for the global ESS state grid
 - Status: backlog
- Plenty of manual tests were done up to now



icshwi / timnet

<> Code Issues 0 Pull requests 0 Actions

MRF based timing network toolkit.

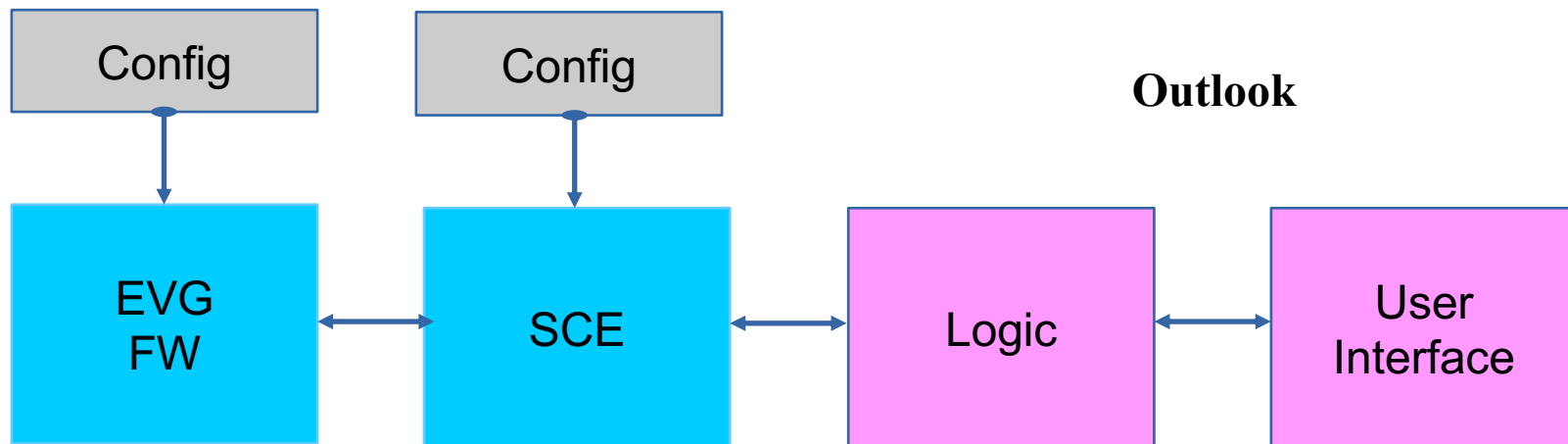
mrf timing **ess** mtca net network Manage topics

18 commits 1 branch 0 packages

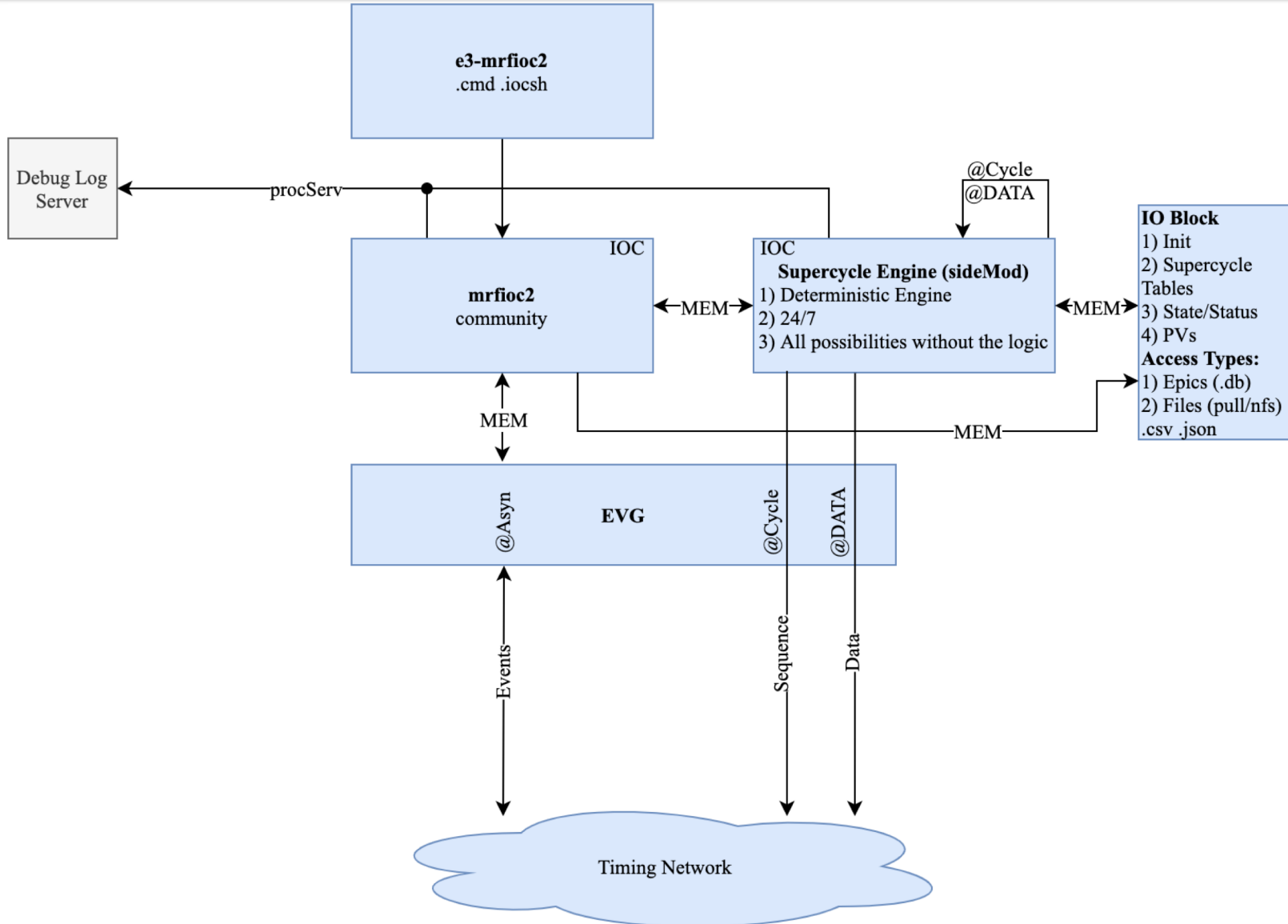
Under development

Supecycle

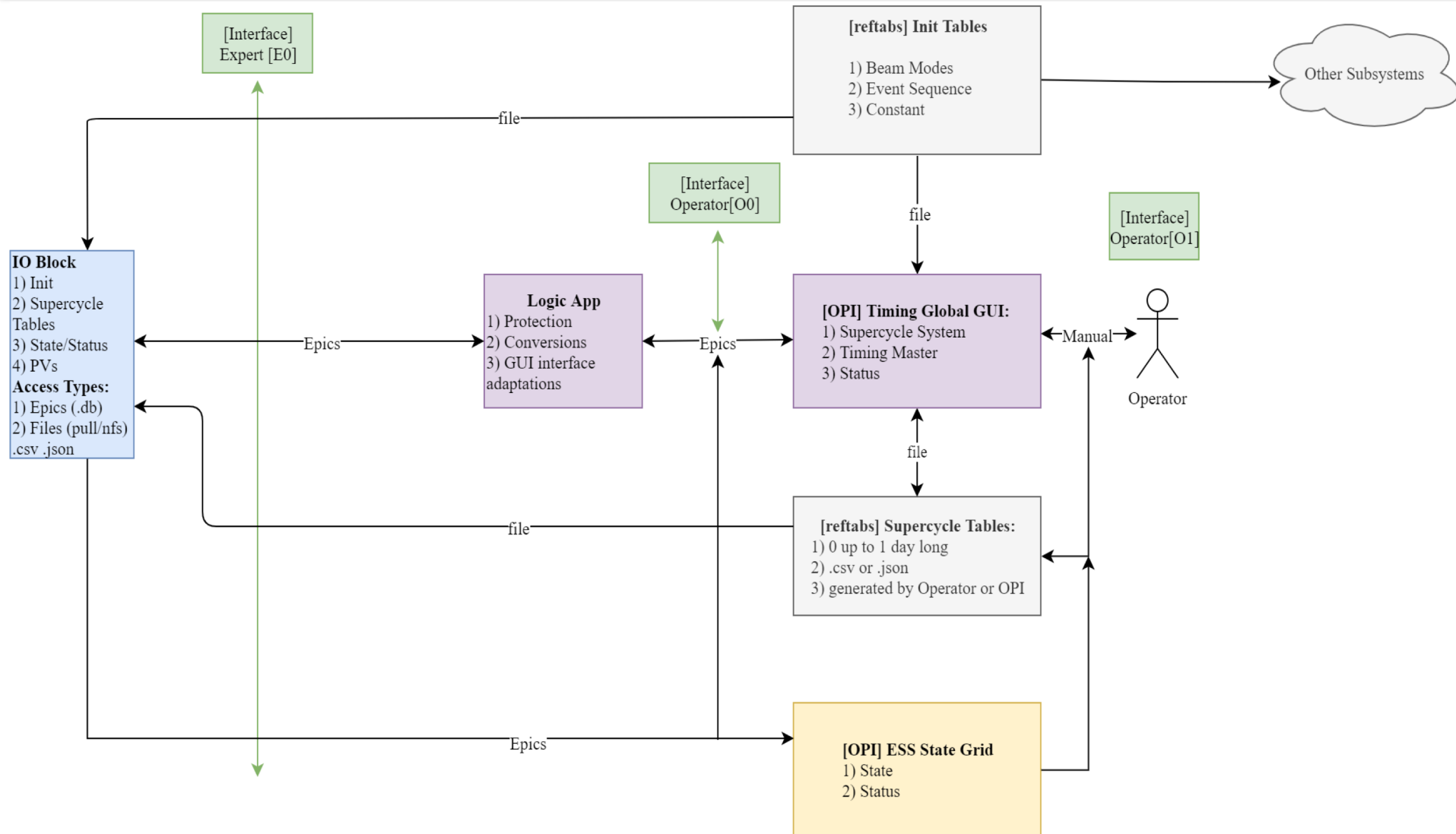
- The supercycle performs:
 - Master Event Sequence Distribution
 - ION_ST, ION_END, BPULSE_ST, BPULSE_END, 14HZ(always), BPULSE_CM
 - Data Buffer Distribution
 - IdCycle, PBCfg, PBDest, PMod, PBLen, PBen, PBCurr, TgRast, TgSeg
- Specification
 - Operating frequency: one linac cycle (14 Hz)
 - Sequential execution



Supercycle Engine (TD-M)



Supercycle Front End - Outlook



Init (Global)

Search or jump to...

icshwi > reftabs > Repository

master reftabs / init / databuffer-ess.json

Find file Blame History Permalink



Modes - refactoring.
Jerzy Jamroz authored 1 week ago

28445ce5

databuffer-ess.json 4.51 KB

Edit Web IDE Replace Delete

```
1 {
2   "ProtNum": 1,
3   "ProtVer": 1,
4   "PBMod": {
5     "None": {
6       "id": 0,
7       "events": "None",
8       "description": "No Beam"
9     },
10    "Conditioning": {
11      "id": 10,
12      "events": [
13        "ION_ST",
14        "ION_END",
15        "DATA"
16      ],
17      "description": "Plasma production, magnetron allowed but no extraction HV"
18    },
19    "ProbeBeam": {
20      "id": 20,
21      "events": [
22        "ION_ST",
23        "ION_END",
24        "DATA"
25      ],
26      "description": "First beam through a particular section; non-damaging even in the case of total beam loss (even repeated); used to verify that machine is ready for operation"
27    },
28    "FastCommissioning": {
29      "id": 30,
30      "events": [
31        "ION_ST",
```















































SCTable Example

A1 = | Id

	A	B	C	D	E	F	G	H	I
1	Id	PBMod	PBDest	BPULSE_ST	BPULSE_END	PBCfg	PBLen	PBEn	PBCurr
2	1	Conditioning	ISrc	0	50	1	1000	100	100000
3	2	Conditioning	LEBT	50	100	1	1001	101	100001
4	3	Conditioning	MEBT	100	150	1	1002	102	100002
5	4	ProbeBeam	ISrc	150	200	1	1003	103	100003
6	5	ProbeBeam	LEBT	200	250	1	1004	104	100004
7	6	ProbeBeam	MEBT	250	300	1	1005	105	100005
8	7	FastCommissioning	ISrc	300	350	1	1006	106	100006
9	8	FastCommissioning	LEBT	350	400	1	1007	107	100007
10	9	FastCommissioning	MEBT	400	450	1	1008	108	100008
11	10	RfTest	MEBT	450	500	1	1009	109	100009
12	11	Conditioning	ISrc	500	550	1	1010	110	100010
13	12	Conditioning	LEBT	550	600	1	1011	111	100011
14	13	Conditioning	MEBT	600	650	1	1012	112	100012
15	14	ProbeBeam	ISrc	650	700	1	1013	113	100013
16	15	ProbeBeam	LEBT	700	750	1	1014	114	100014
17	16	ProbeBeam	MEBT	750	800	1	1015	115	100015
18	17	FastCommissioning	ISrc	800	850	1	1016	116	100016
19	18	FastCommissioning	LEBT	850	900	1	1017	117	100017
20	19	FastCommissioning	MEBT	900	950	1	1018	118	100018
21	20	RfTest	MEBT	950	1000	1	1019	119	100019
22	21	Conditioning	ISrc	1000	1050	1	1020	120	100020
23	22	Conditioning	LEBT	1050	1100	1	1021	121	100021
24	23	Conditioning	MEBT	1100	1150	1	1022	122	100022
25	24	ProbeBeam	ISrc	1150	1200	1	1023	123	100023

Workflow

Jira – Mainly ICSHWI-1686

Issues ▾ Boards ▾ BigPicture ▾ Insight ▾ Tests eazyBI Create					
1.	✔ Fanout Firmware Characterization Plan		DONE	Javier Cereijo Garcia	0% 
2.	✔ Fanout Firmware Characterization to MRF		DONE	Javier Cereijo Garcia	0% 
3.	✔ Check the new MRF firmware for the final production		DONE	Javier Cereijo Garcia	100% 
4.	✔ Release mrfioc2 version for ESS		DONE	Jerzy Jamroz	90% 
5.	✔ mrfioc2 iocsh for FOUT preparation		DONE	Jerzy Jamroz	40% 
6.	✔ Build the procedure to switch FOUT to EVM		DONE	Jerzy Jamroz	10% 
7.	✔ Build the ipmiComm EPICS DB definition for EVR/EVM		DONE	Jeong Han Lee [X] (Inactive)	0% 
8.	✔ Define MTCA System for the Timing System		DONE	Jeong Han Lee [X] (Inactive)	100% 
9.	✔ Define Site-Wide Timing System Components		DONE	Jeong Han Lee [X] (Inactive)	0% 
10.	✔ ESS Timing System Deployment HW and physical port number count		DONE	Jeong Han Lee [X] (Inactive)	100% 
11.	✔ Define Timing MTCA Configuration		DONE	Jeong Han Lee [X] (Inactive)	1% 
12.	✔ Order only MRF Hardware in the zero batch		DONE	Peter van Velze	0% 
13.	✔ Order the first batch of MTCA hardware		DONE	Faye Chicken	7% 
14.	✔ Order the first batch of MRF Hardware		DONE	Faye Chicken	7% 
15.	✔ Timing Network Topology for TM and TDs		DONE	Peter van Velze	62% 
16.	✔ Timing Network Topology for Event Receiver		DONE	Jeong Han Lee [X] (Inactive)	64% 
17.	✔ Lab test for TM/TD MTCA System		DONE	Jerzy Jamroz	100% 
18.	✔ System integration HW and SW for the initial SAT release		DONE	Jerzy Jamroz	30% 
19.	Setup TM/TD MTCA System		IN PROGRESS	Jerzy Jamroz	
20.	✔ EVM issues and new img 207.8 evaluation		DONE	Jerzy Jamroz	100% 
21.	✔ [Timing] Review of the machine operation modes, events, configs		DONE	Jerzy Jamroz	100% 
22.	✔ Test new mTCA EVR features		DONE	Jerzy Jamroz	100% 
23.	✔ Timing Smoke Test - ESS production based		DONE	Jerzy Jamroz	100% 
24.	Estimate the global target delay		BACKLOG	Jerzy Jamroz	

Conclusions

- The installation is the main concern at the moment.
- NCL part will validate the workflow and tools.
- The supercycle engine will accept any input data (expert access) to the timing system – operators will have the full freedom.
- The commissioning experience will be a base for the supercycle front end development (logic and GUI).
- „reftabs” repository will serve the settings for other subsystems as well.