Automatized RF Conditioning Application

Emmanouil Trachanas
Electrical and Computer Engineer
European Spallation Source
Emmanouil.Trachanas@esss.se

Thomas Fay
Control Systems Engineer
European Spallation Source
thomas.fay@esss.se

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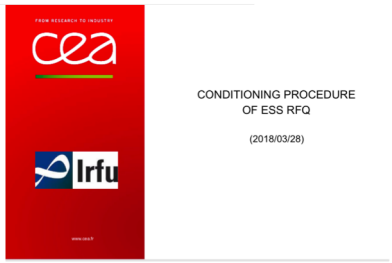
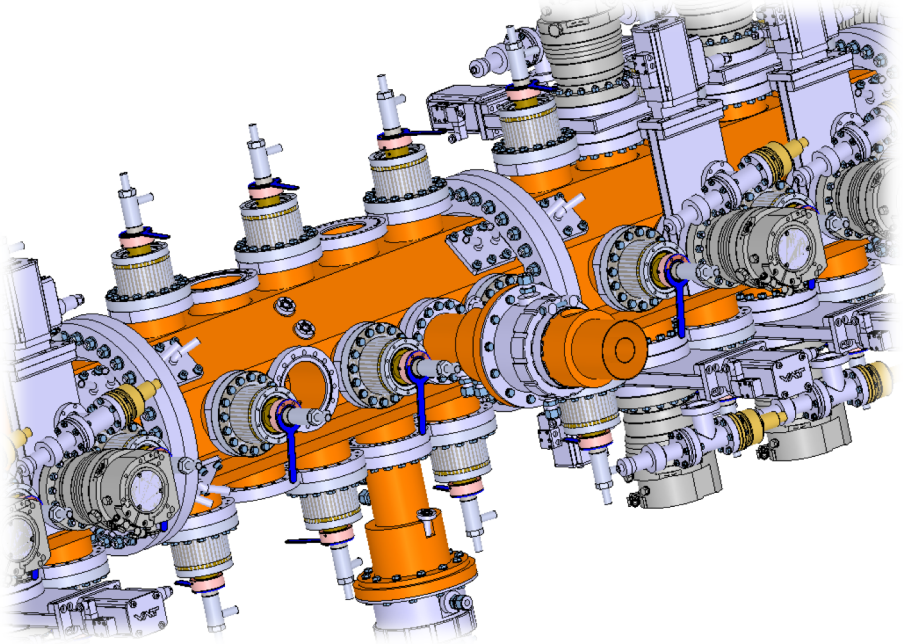
Scope of the project

”Create a EPICS/IOC application implementing the algorithm for the automatized RF conditioning procedures of NCL cavities ”



Grateful to **Alexis Gaget** and other colleagues for the base code and assistance during integration



Application Characteristics

Algorithm Implemented on SNL

- Code integration and Modification
- **EPICS modules provided by CEA**

OPI created on BOY editor of CS studio

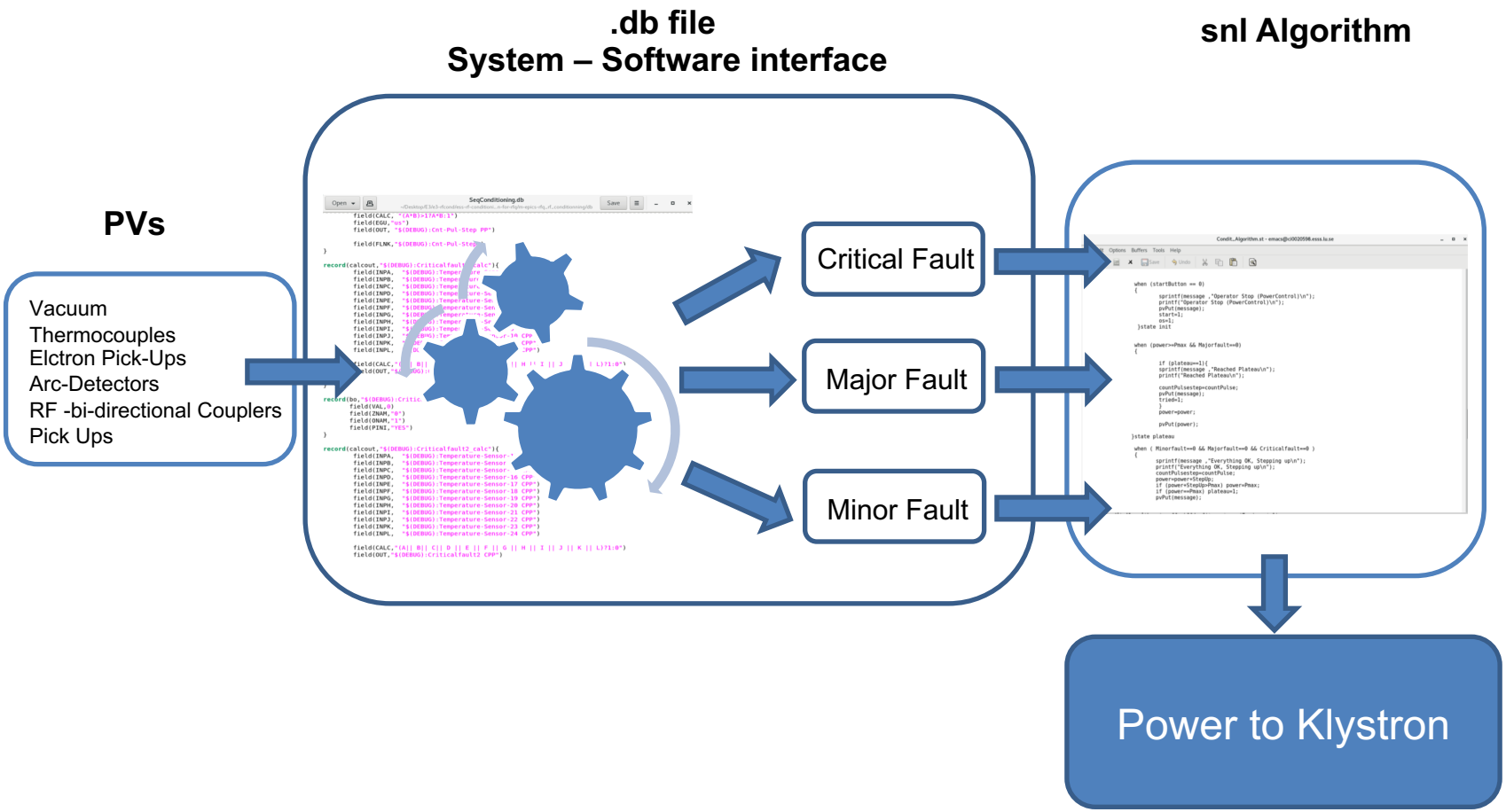
One centralized menu with 2 tabs

- ✓ Configurable Cycle
- ✓ Threshold Input
- ✓ Work with Interlock IOC
- ✓ Generalized module for flexibility

The application sets the klystron power and its parameters and reads PVs as response and clasifies possible errors with severity (Minor-Major-Critical)

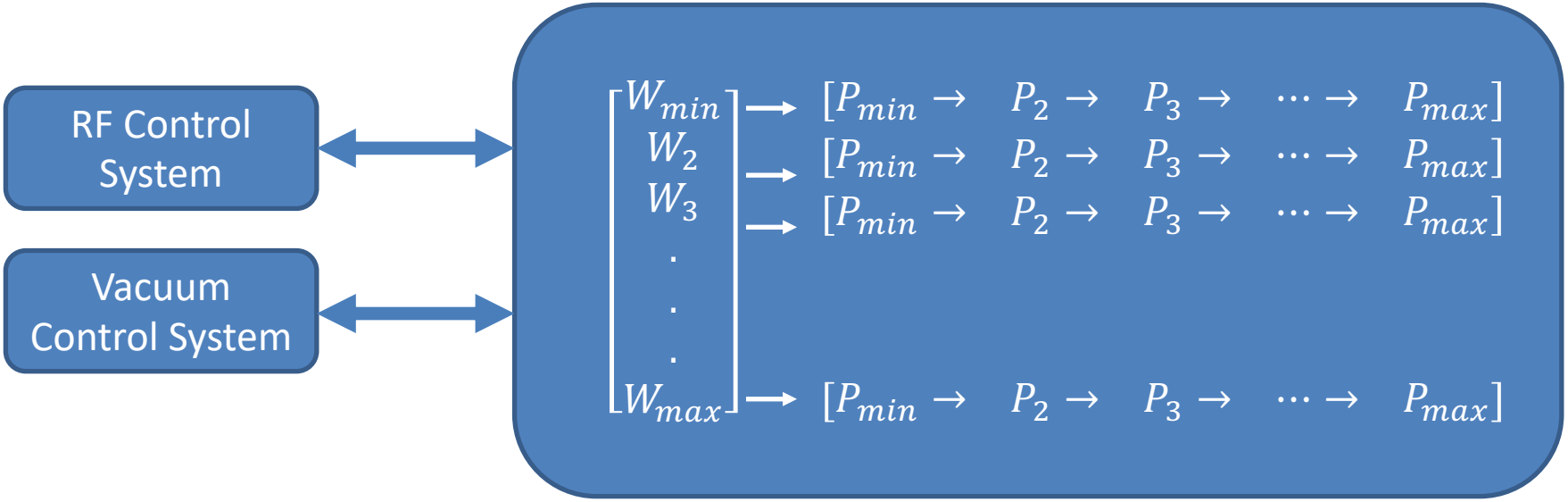
Depending on the fault, power stays the same or decreases. In case of critical fault RF LPS shuts power down until fault is corrected.

IOC Architecture

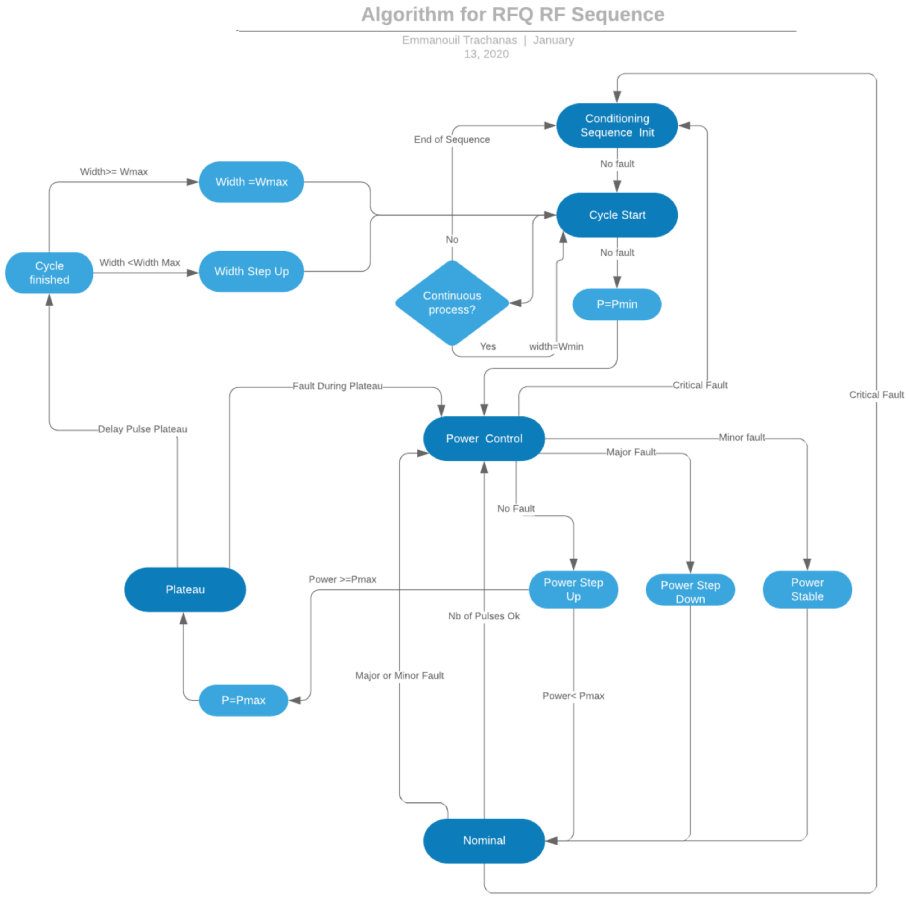


Conditioning Method

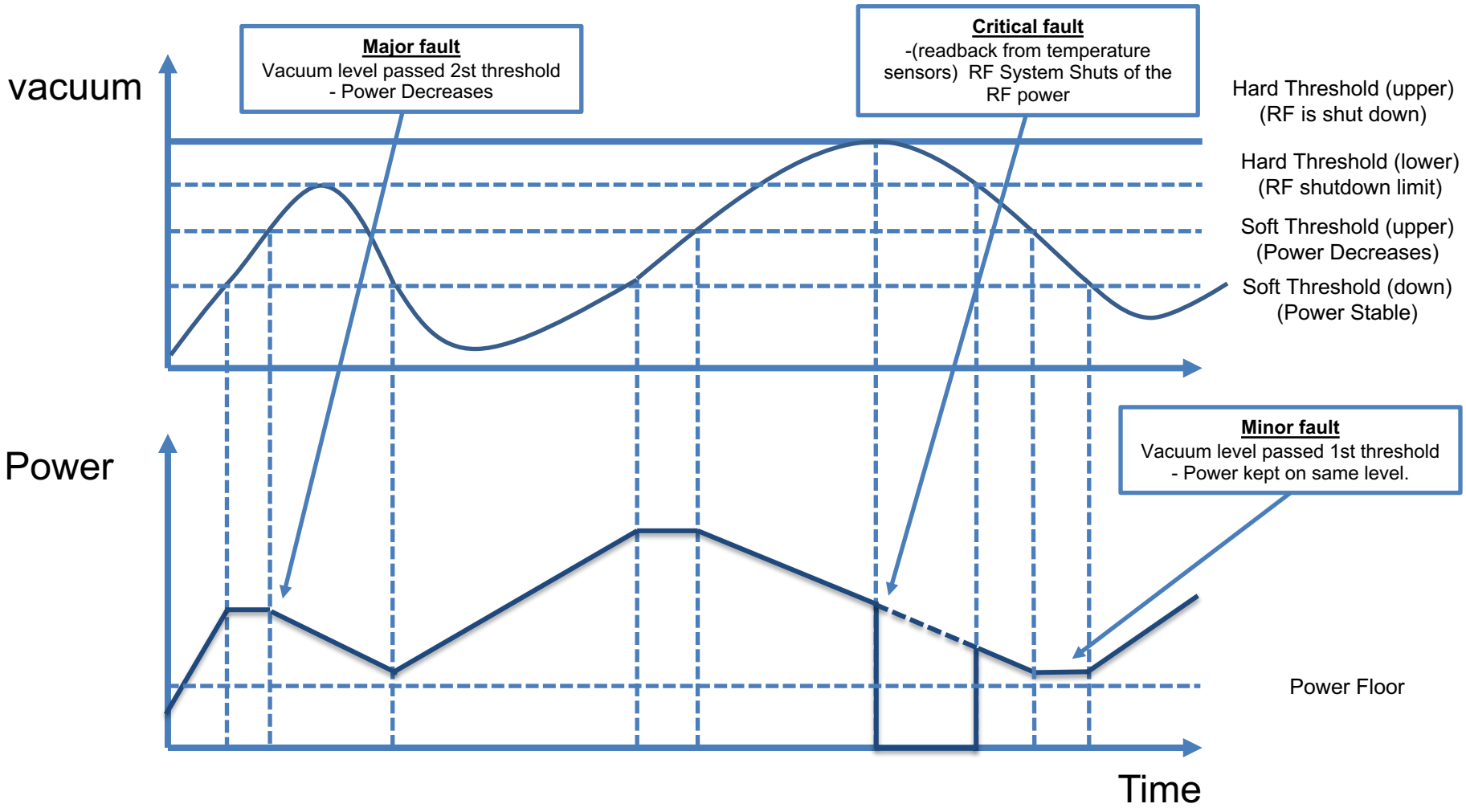
We define the pulse width vector **W**= [w_{min} ,w_2, w_3, ... w_{max}] .Each w_i constitutes a cycle and a power vector **P**= [P_{min} , P_2, P_3 .... P_{max}] is assigned to each cycle. Each value of the power vector is assigned to the klystron (for a number of pulses) and the readback of vacuum and RF interlocks is checked . **Depending if there is an interlock or not power is set accordingly**. Before reaching the next cycle P_{max} is assigned for a given amount of time (plateau)



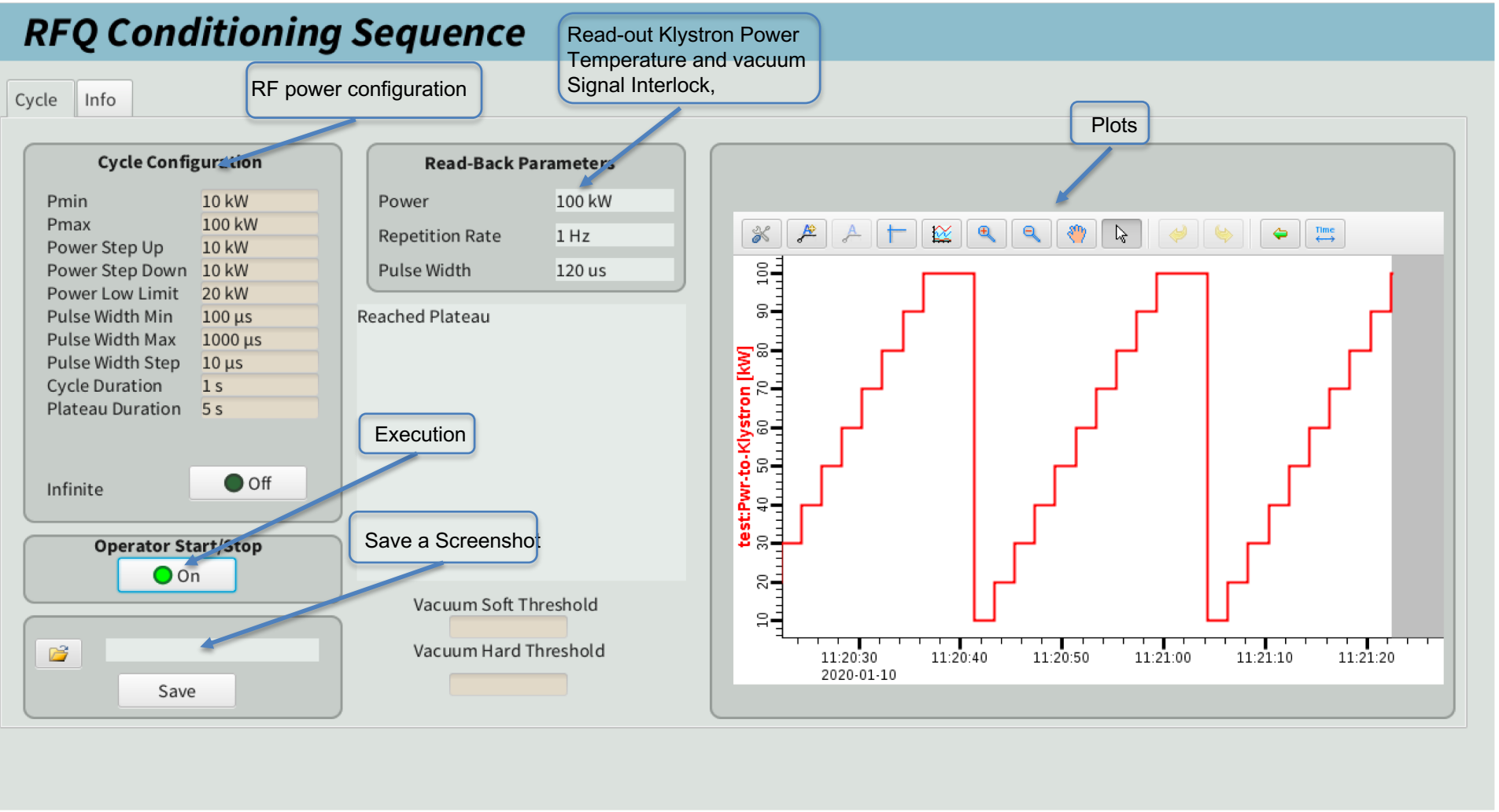
Algorithm Flowchart



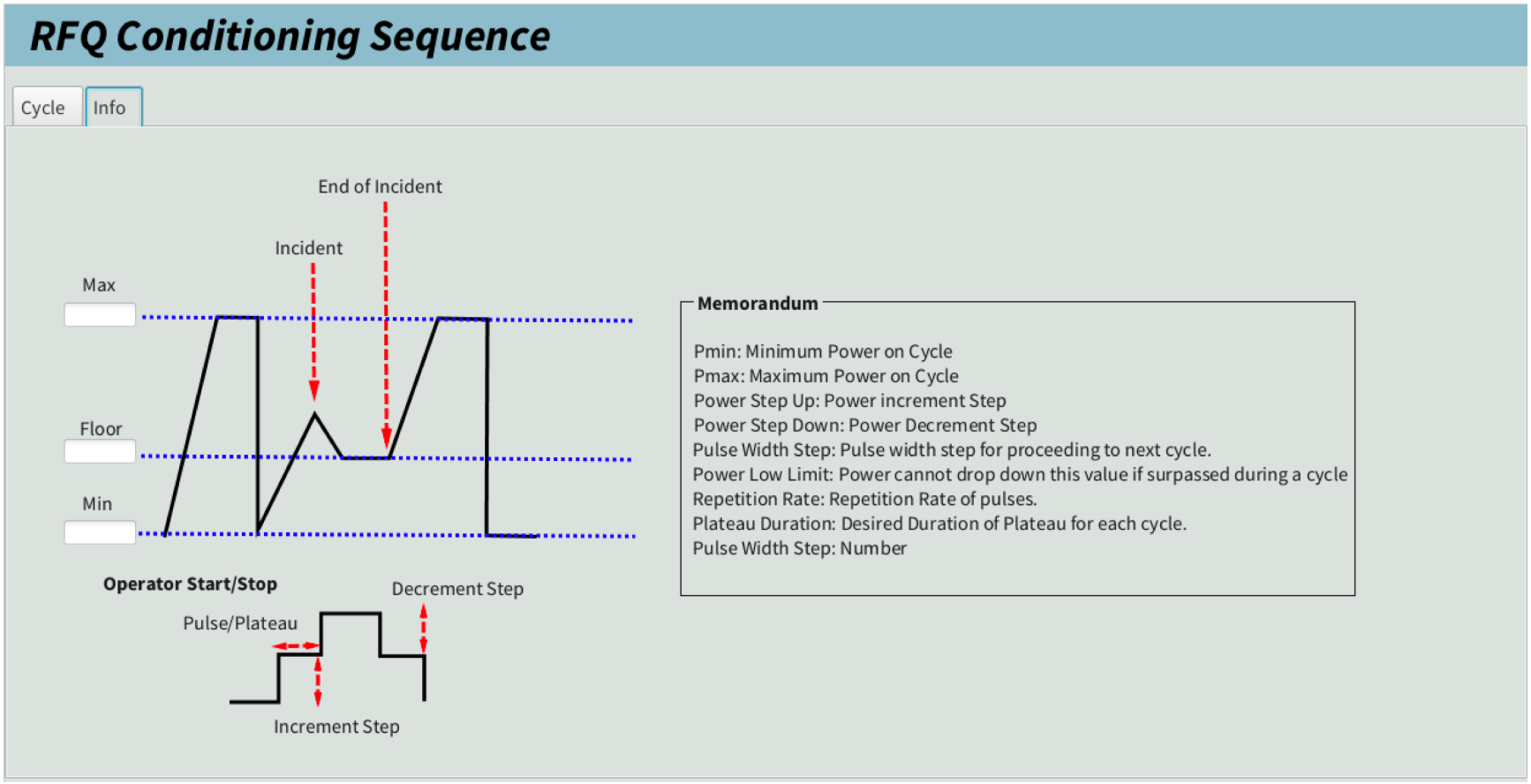
Example


vacuum
Major fault
Vacuum level passed 2st threshold
- Power Decreases
Critical fault
-(readback from temperature sensors) RF System Shuts of the RF power
Hard Threshold (upper)
(RF is shut down)
Hard Threshold (lower)
(RF shutdown limit)
Soft Threshold (upper)
(Power Decreases)
Soft Threshold (down)
(Power Stable)
Power
Minor fault
Vacuum level passed 1st threshold
- Power kept on same level.
Power Floor
Time

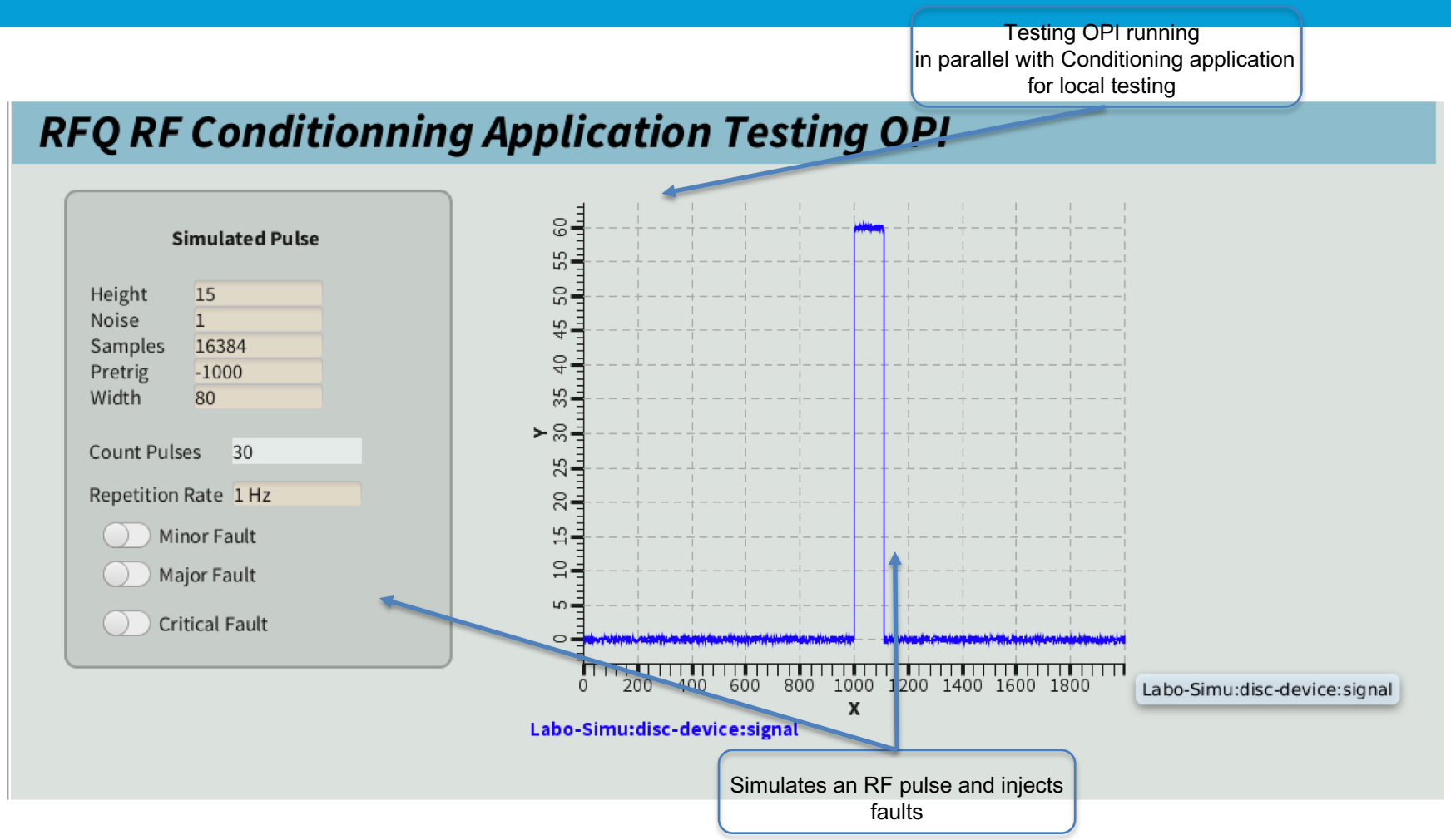
Application Menu (1/3)



Application Menu (2/2)



Testing EPICS module



Status And Future Steps

- ✓ Design of OPI -DONE
- ✓ Algorithm Integrated
- ✓ Set-up mock up functional environment.

✓ Milestone I

- ✓ Local Tests for algorithm verification
- Manual and Documentation On going

Milestone II

- Integrated Tests (Test stand 2 as a first step)
- List of PVs from Control Systems
- Creation of Generic module

Milestone III

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