Status of the VMM3a integration

IKON 18
Lund

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Overview

- What is the VMM3a ?
- VMM3a imaging features
- VMM3a rate features
- Integration of RD51 VMM3a hybrid into ESS readout

VMM3a ASIC

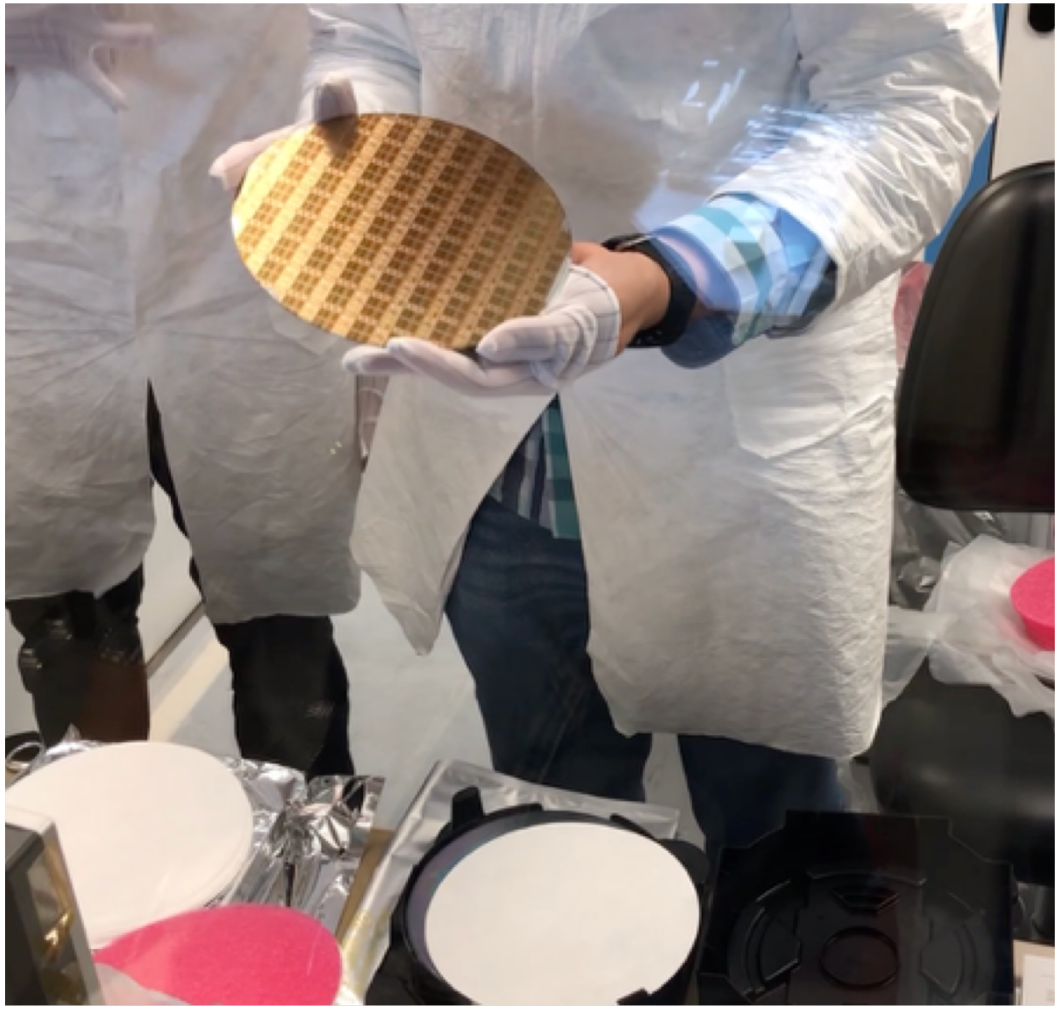
- VMM3a is an ASIC developed by Brookhaven National lab for the ATLAS New Small Wheel upgrade at CERN
- ASIC developed to read out Micro Pattern Gaseous detectors
- Huge interest from labs around the world to use the chip

- Since NMX uses a MPDG (Gd-GEM detector), VMM3a natural choice
- In 2018 it has been shown at ESS that chip can also be used for other gas detectors like Multi-Grid (analog and digital data taken) and Multi-Blade (analog matching successful)
- VMM3a is the electronics choice to readout the NMX, CSPEC, ESTIA, TREX and FREIA detectors

VMM3a ASIC

Wafers

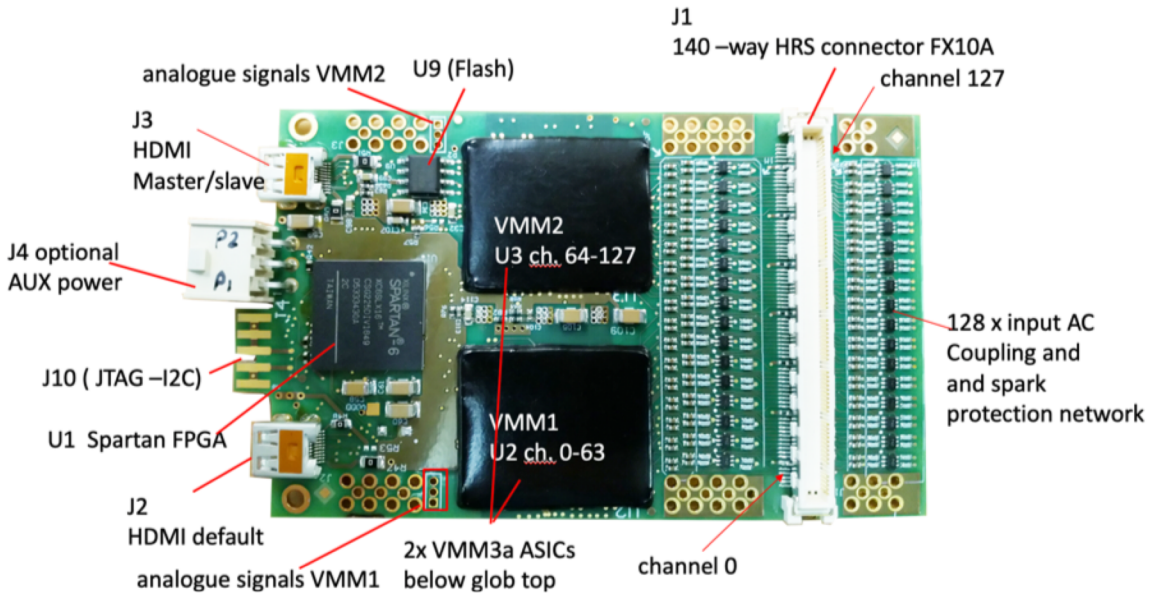
- RD51 received 25 wafers in August, 10 of which belong to ESS
- 3 wafer diced for test production of 160 RD51 hybrids
- 40 hybrids of the 160 are for ESS
- expected in March
- if yield sufficiently well, production of hybrids from remaining wafers to follow

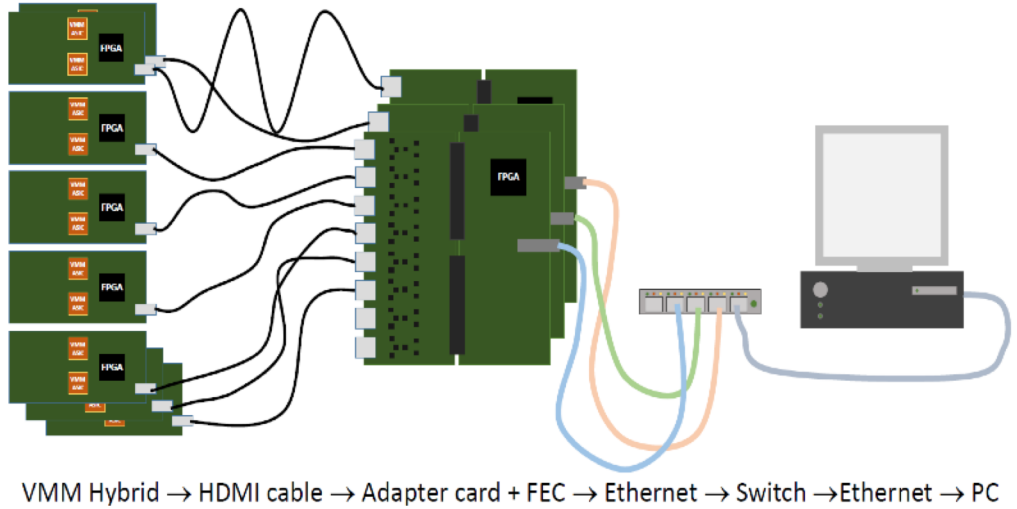


RD51 VMM3a hybrid

Integration into the SRS during Brightness

- Common ESS-CERN project, successful integration of the VMM3a ASIC into the Scalable Readout System (SRS) by Michael Lupberger (now at Bonn University)
- Hybrid firmware at the moment optimized for speed and documented by Marek Hracek (financed by ESS and CERN) and Bonn University
- NMX in-kind agreement signed with University of Talin in Estonia for firmware development and electronics (kick-off March 24th)



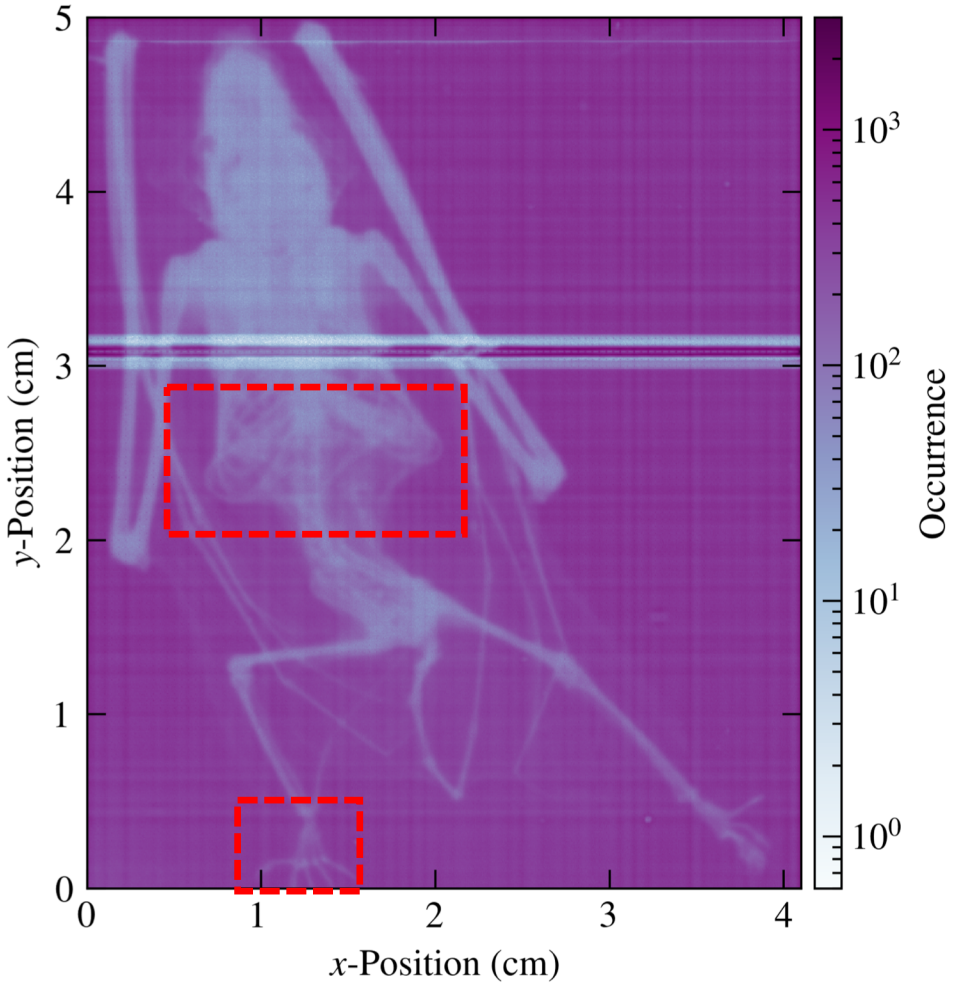


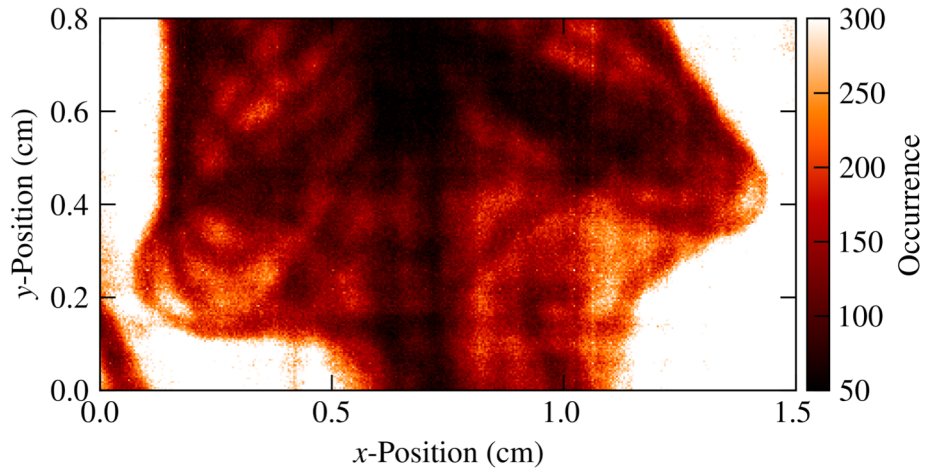
VMM Hybrid → HDMI cable → Adapter card + FEC → Ethernet → Switch →Ethernet → PC

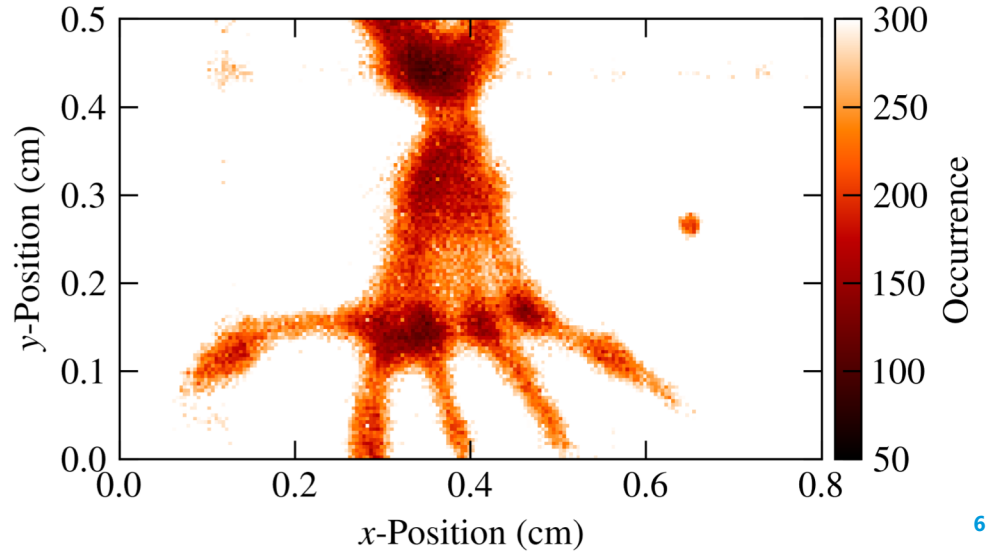
X-ray imaging at high rates

4.2 x 10^8 clusters, acquired in 35 minutes (200 kHz rate)

X-rays are easily available, energy deposit similar to NMX Gd-GEM

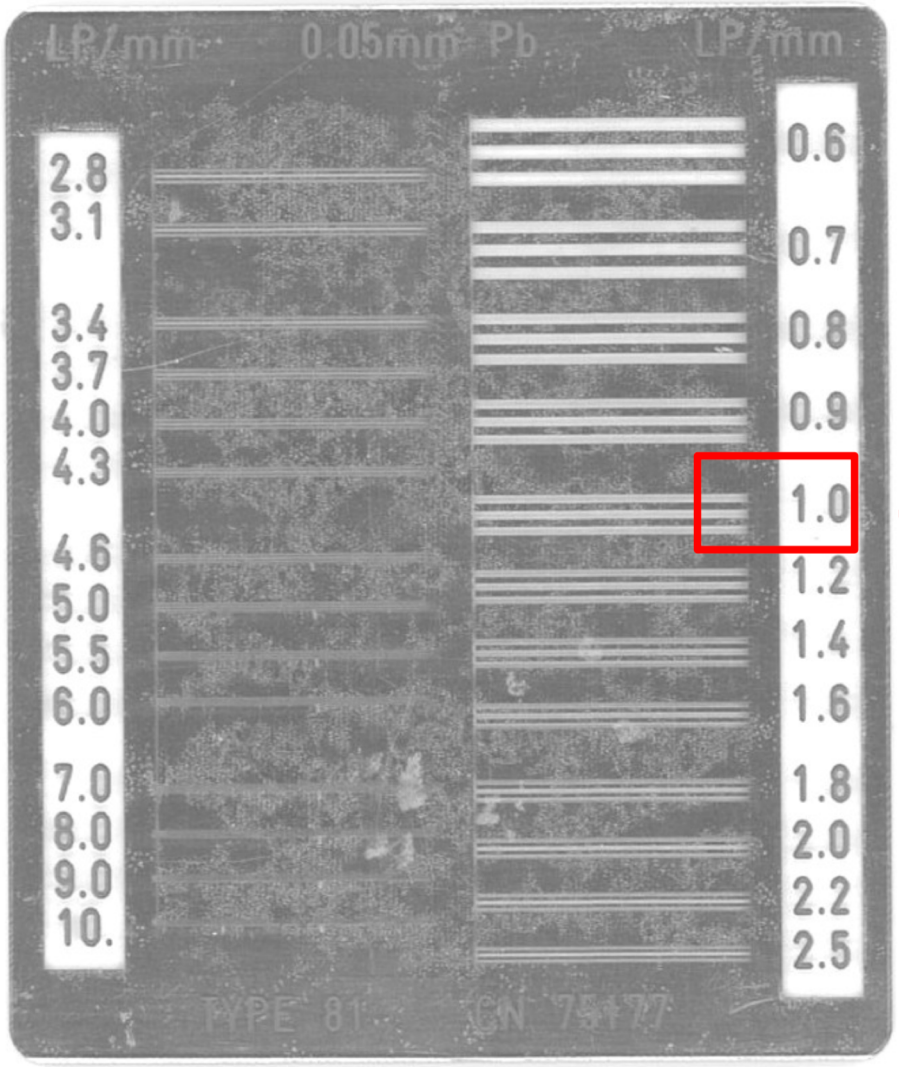




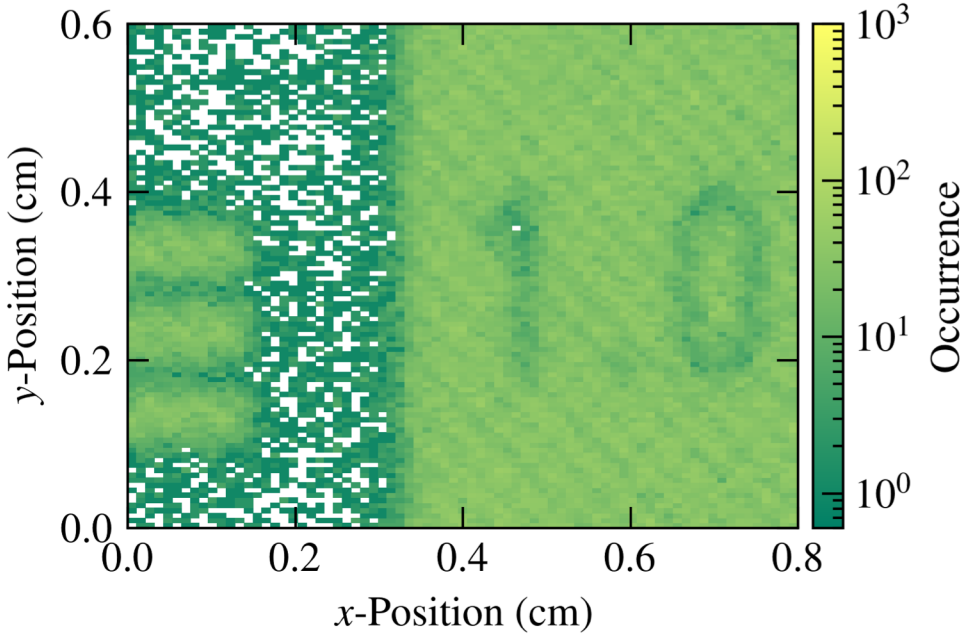


High resolution X-ray imaging

VMM3a is capable ASIC and produces VERY good quality data.

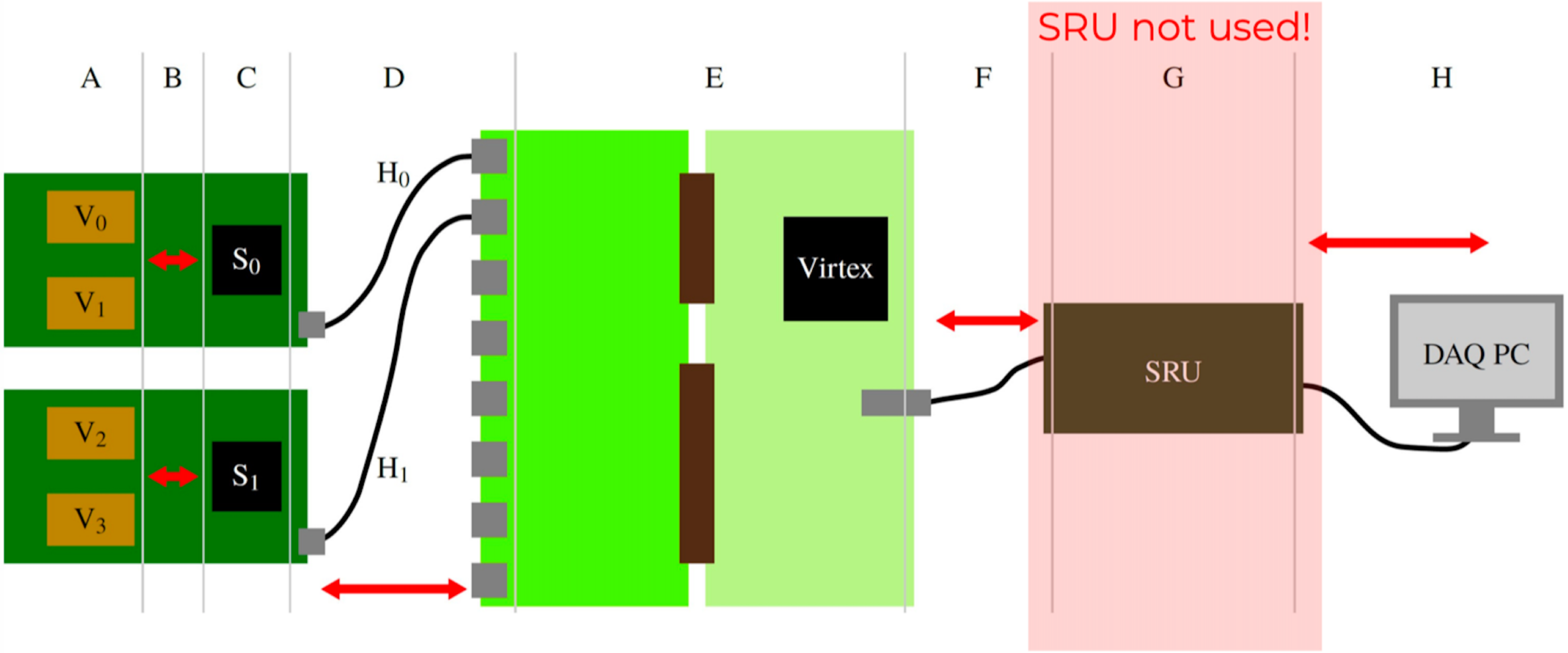


The ASIC is successful. Therefore we can use it for our detectors



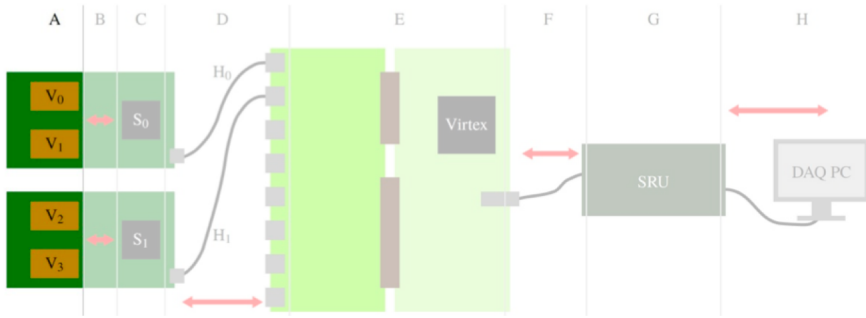
VMM3a rate measurements

SRS (Hans Muller @CERN) test and development system for ESS



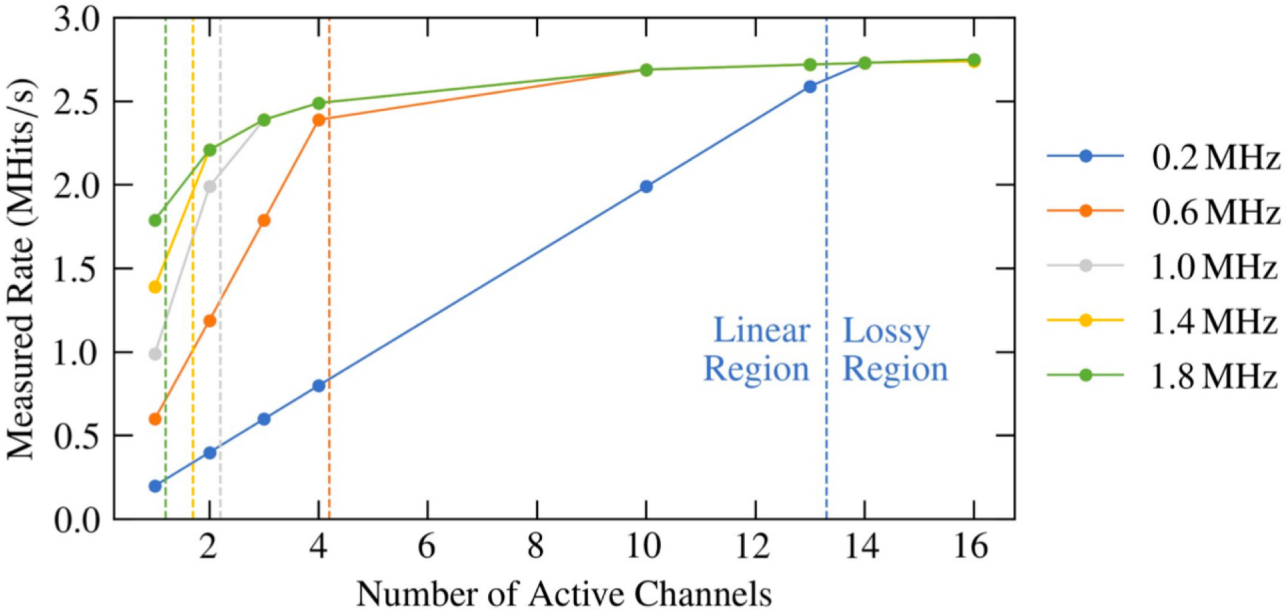
VMM3a rate measurements

ASIC



A: Multi Channel Stability

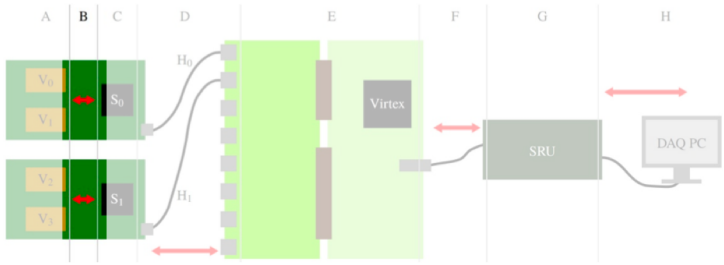
Study the digital data
→ output rate depending on input frequency and active channels



- All channels are pulsed with the same frequency
- Channels have always equal number of hits in linear region (left of dotted line) and in lossy region (right of the dotted lines)
- Losses are thus equally distributed over all channels

VMM3a rate measurements

ASIC – Spartan 6



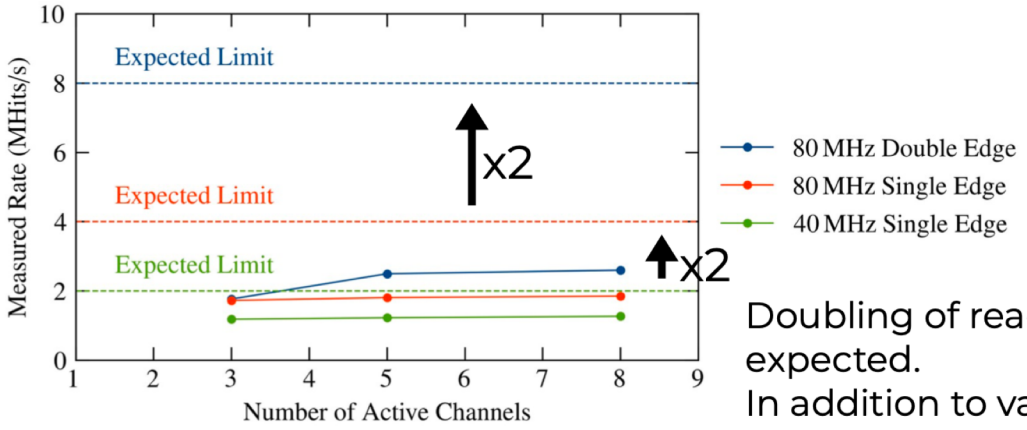
B: Readout Speed

Expected:

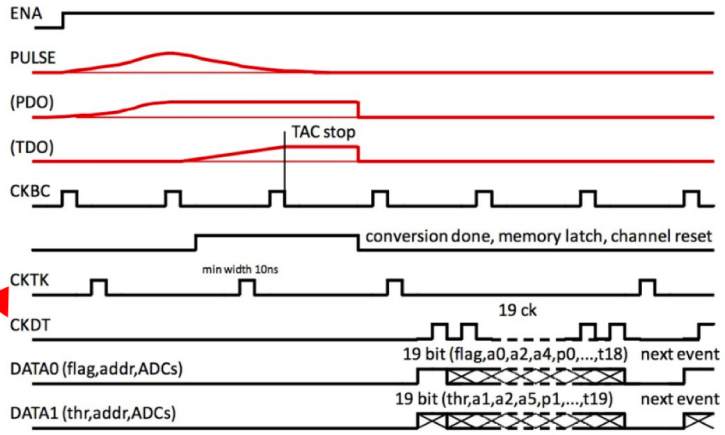
- Max. 160 MHz readout clock
- 2 Data lines per channel
- Dual edge readout
- **Max. 640 Mbps = 16 MHits/s output**

Measured:

- Stable operation only up to 80 MHz dual edge clock possible, so **max. 320 Mbps = 8 MHits/s output**
- **Team in Bonn is working on this**



Doubling of readout rates expected.
In addition to variable CKDT fixed CKTK @ 40 MHz

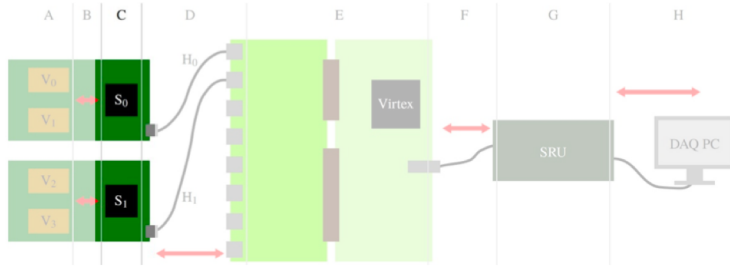


[VMM3a Manual]

VMM3a rate measurements

Spartan 6

C: Spartan®-6 FPGA

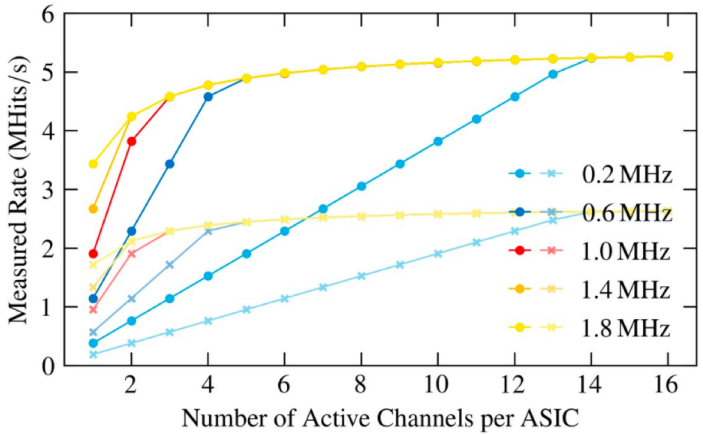


Expected:

- Max. output rate:
  950 Mbps = 23.75 MHits/s

Measured:

- Data rate from 1 to 2 VMMs doubles
- **216 Mpbs = 5.4 MHits/s**



1 VMM

2 VMMs

Data rate scales by a factor of 2

Data losses are symmetrically distributed

VMM3a rate measurements

Summary

With present firmware and settings available:

- 2.7 Mhits/s or 110 Mbit/s per VMM3a ASIC

With upgraded firmware

- 8.0 Mhits/s or 320 Mbit/s per VMM3a ASIC
- Test by DMSC show that the EFU can deal already deal with 17 Mhit/s

Theoretically higher rates possible, under investigation

For further planning of instrument readouts, the rate of 320 Mbit/s per VMM3a or 640 Mbit/s per RD51 hybrid (2 ASICs) should be used to determine the necessary number of assister cards

=> No bottlenecks detected in the readout chain from VMM up to DMSC

Integration into ESS readout

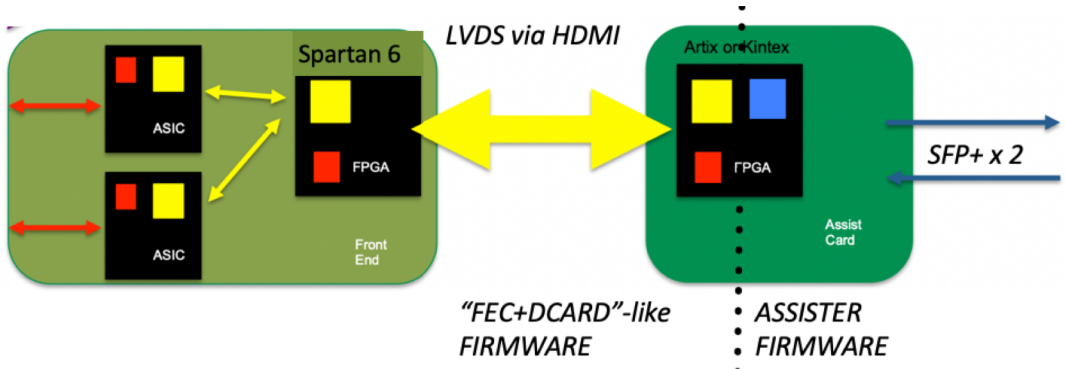
RD51 hybrid -> Assister

Road map hybrid:

- For first integration tests, use existing RD51 VMM3a hybrid with Spartan 6
- Help to improve readout speed of RD51 hybrid firmware
- Structure, clean up and document the firmware
- Later on, replace as a common RD51 effort Spartan 6 with 7 series FPGA

Road map assister:

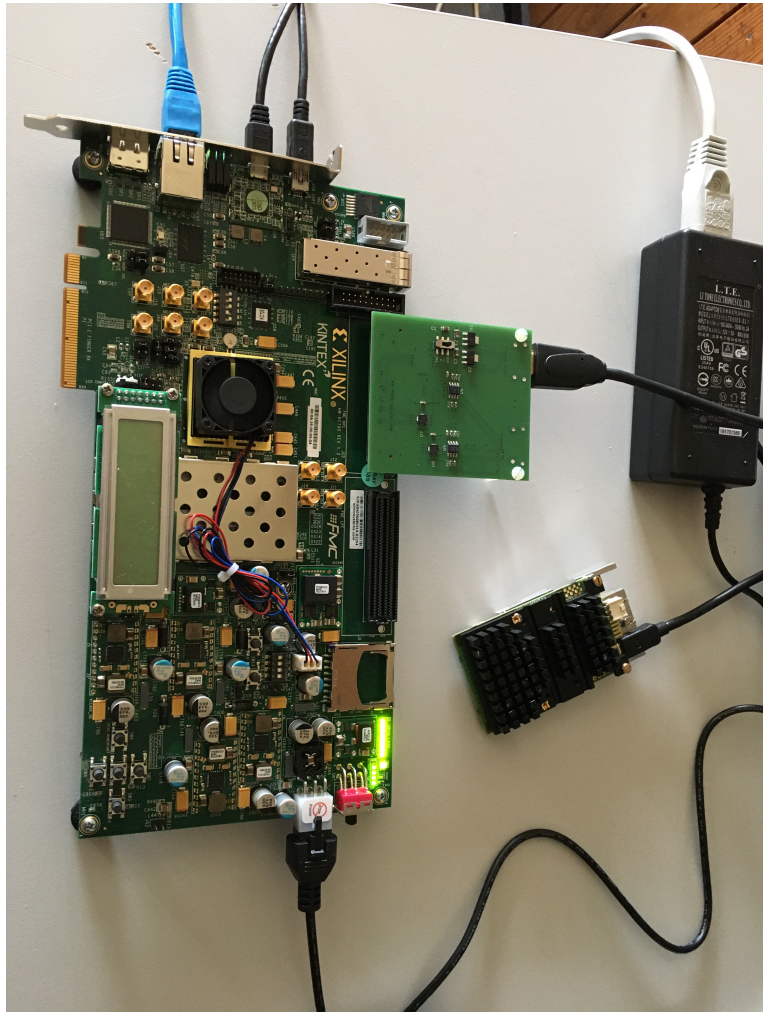
- Use **Xilinx Kintex-7 FPGA KC705 Evaluation Kit** as assister platform
- Design FMC to HDMI adapter (mini version of DVM card) to connect two hybrids
- Develop firmware for assister (in principle, port existing Virtex6 FEC firmware to assister Kintex 7)



Integration into ESS readout

RD51 hybrid -> Assister

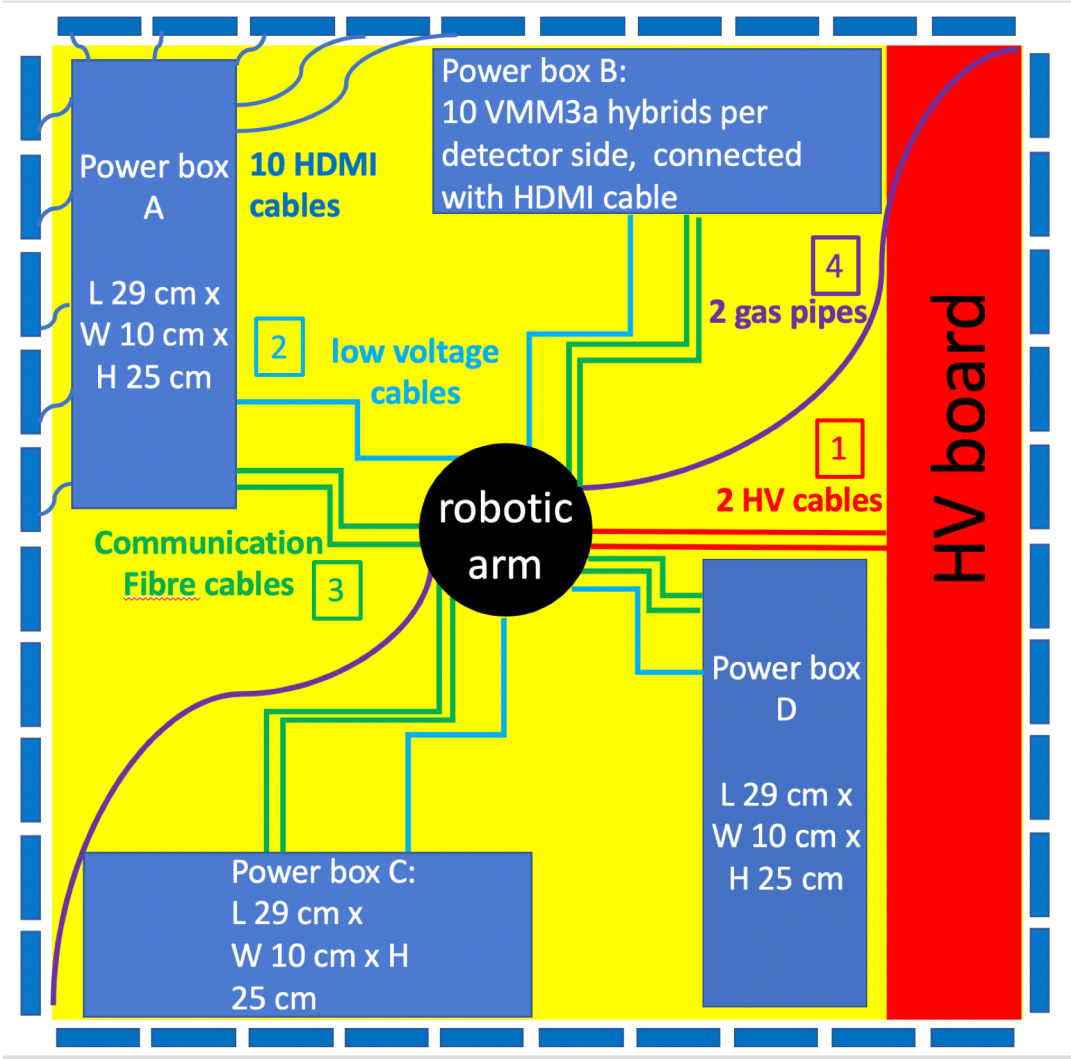
- Adapter card connects two RD51 hybrids to the FMC connector of the Kintex KC705 evaluation board
- Card tested at the moment
- Steven and me started to port Virtex6 firmware to Kintex7 (work expected to take 3 months)
- Virtex 6 firmware rather complex and not documented, but making progress in understanding
- Aim is to be able to have a working prototype at the next IKON



Integration into ESS readout

Typical details encountered during integration

- Will the combination of Xilinx KC705 and adapter card be final ?
- Space requirements very large for this solution, which might be a challenge for some instruments
- Powering concept needed, the present adapter card does not power VMMs (1.75 V at 1.6 A, 3 V at 0.14 A, 3.3 W per hybrid)
- Thermal budget/cooling has to be considered
- Ground and cable details to be determined
- These are the typical details we expect to solve during each integration steps



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