ESS Modulator Workshop
April 24, 2012

HVCM Modulator Performance, Upgrades & Plans

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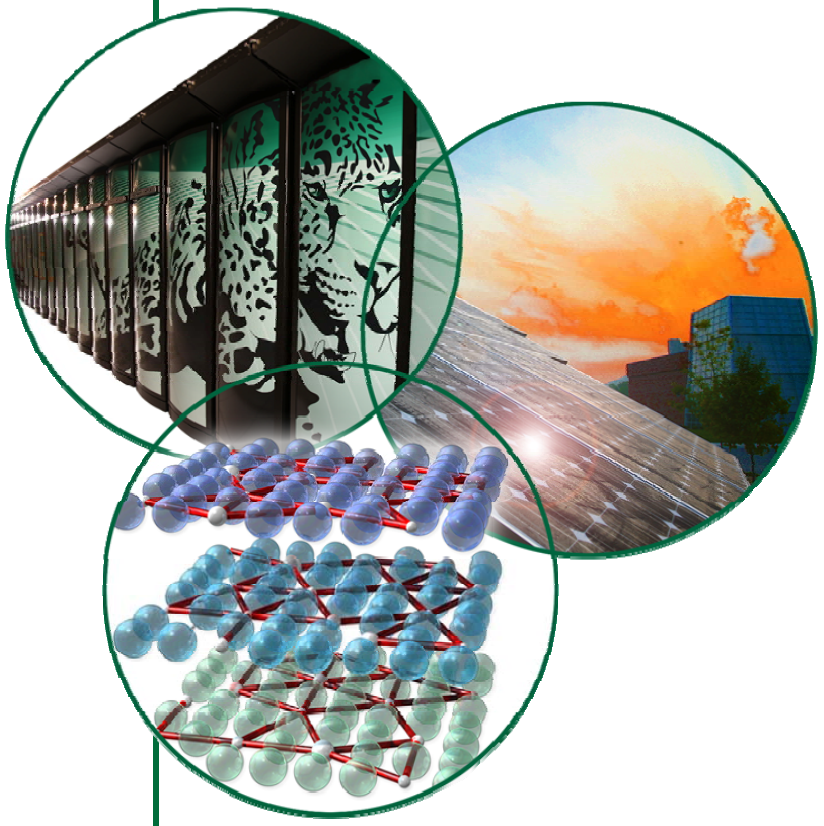

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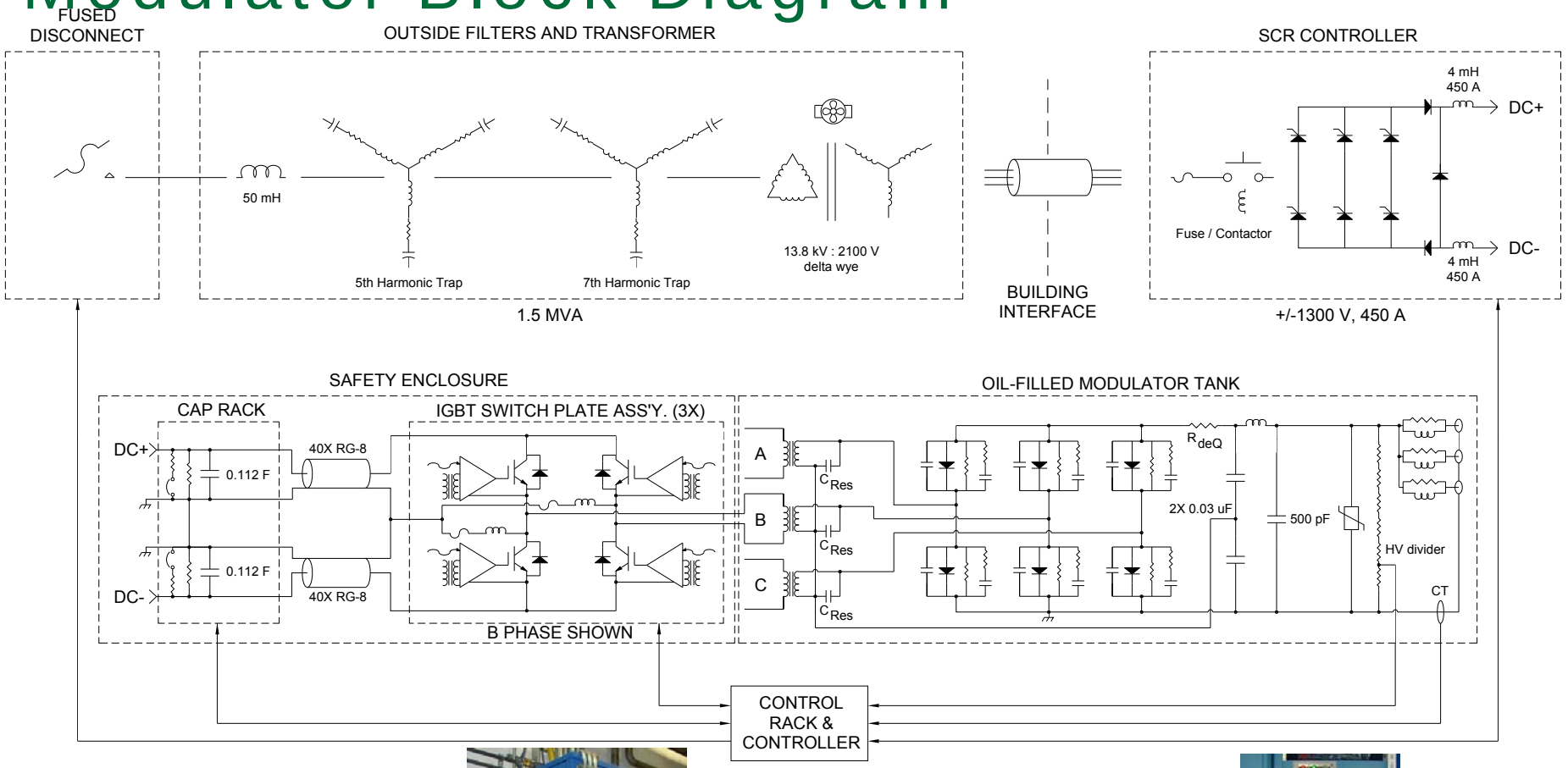
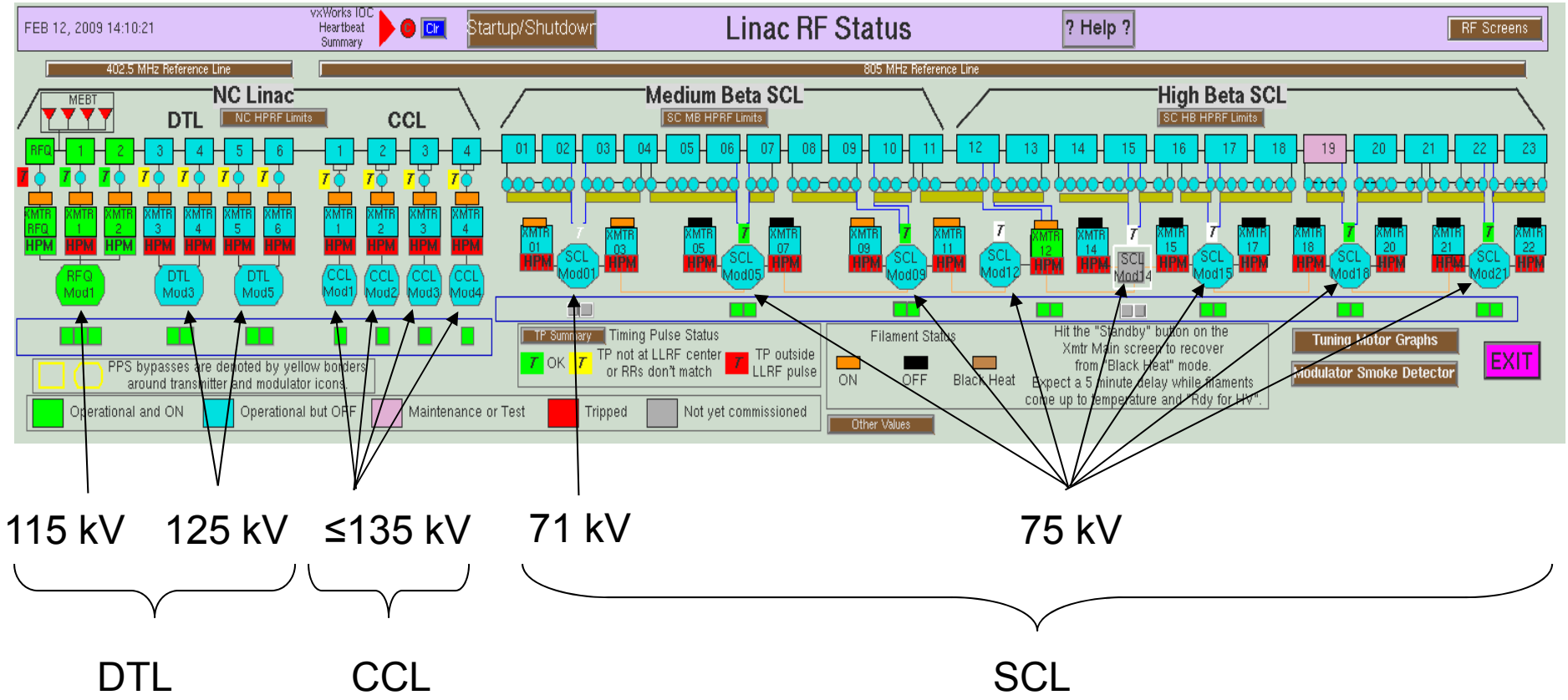
Modulator Block Diagram



Cavity/Klystron/Modulator Layout



115 kV 125 kV ≤135 kV 71 kV 75 kV

DTL CCL SCL

- 15 modulators: 3 - DTL, 4 - CCL, 8 – SCL (1 added 2008)
- Multiple HVCM/Klystron Configurations

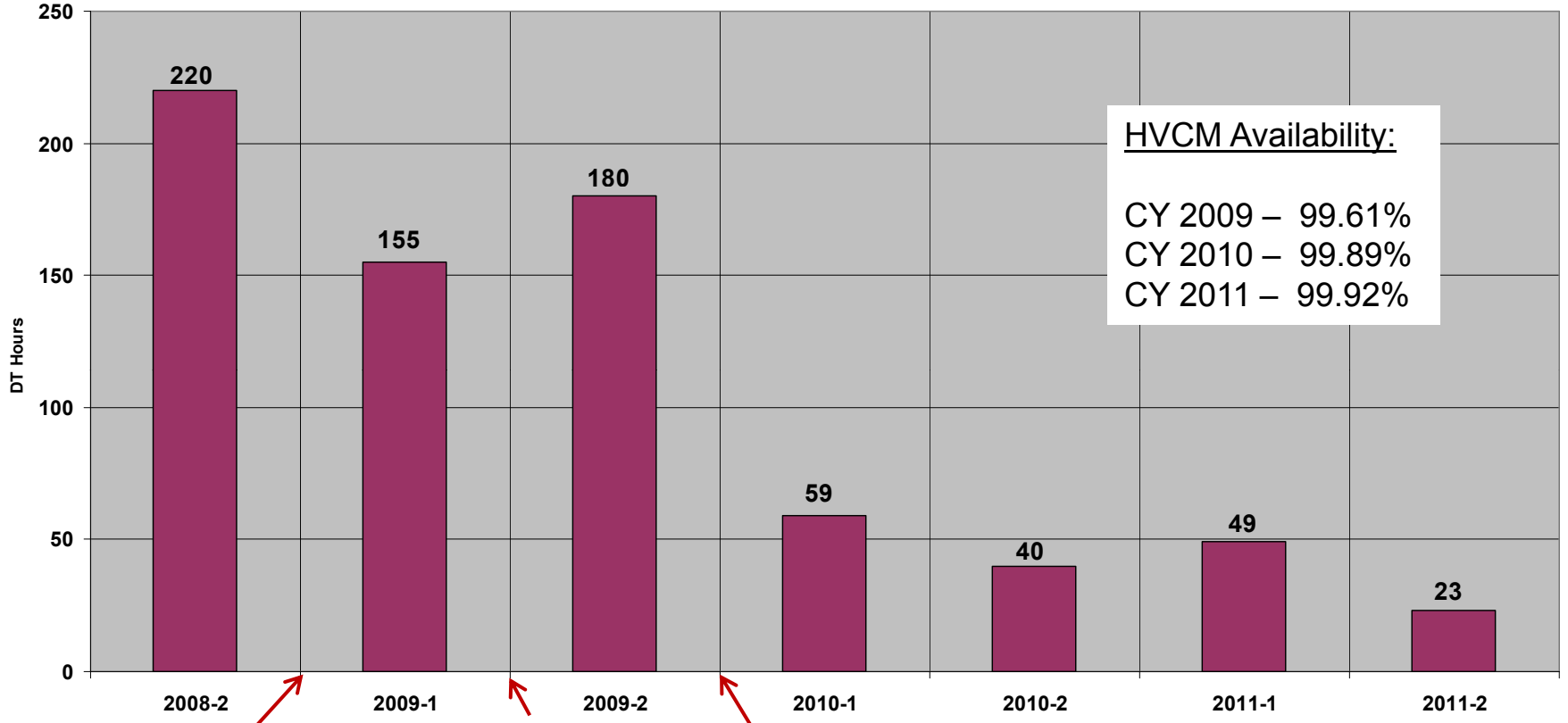
Outline

- Performance & Past Upgrades
- UPGRADE – Controls and Alternate IGBT Gating
- UPGRADE – IGBT snubbers
- Alternate topology

Operational Parameters

Modulator	Operation hours (as on 12.22.2011)	Load: # of klystrons	V mod, (kV)	I mod, (A)	P peak, (MW)
DTL-1 (RFQ)	43,091	3	115	92	10.6
DTL-3	40,279	2	125	72	9.0
DTL-5	40,231	2	125	68	8.5
CCL-1	38,953	1	128	68	8.7
CCL-2	36,354	1	131	64	8.4
CCL-3	38,203	1	135	67	9.0
CCL-4	36,223	1	126	72	9.1
SCL-1	37,974	11	71	124	8.8
SCL-5	38,044	10	75	109	8.2
SCL-9	36,461	10	75	106	8.0
SCL-12	37,685	10	75	109	8.2
SCL-14	18,871	10	75	109	8.2
SCL-15	36,652	10	75	114	8.5
SCL-18	36,954	10	73	112	8.2
SCL-21	33,248	10	75	108	8.1
	549,223				

HVCM Downtime Hours by Runs



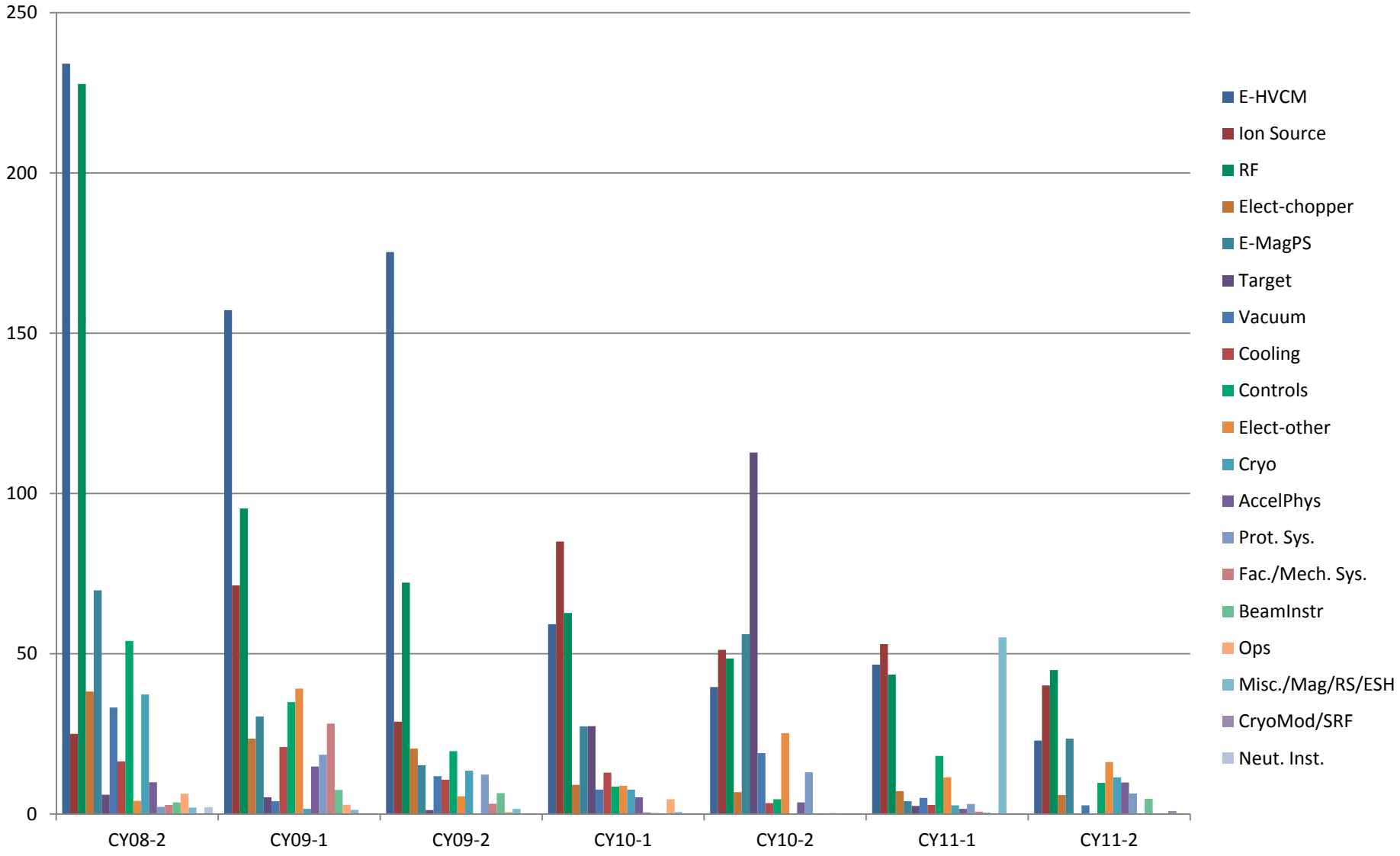
•60 Hz Operation begins here
•New SCL HVCM installed (10% power reduction)

•IGBT timing changes implemented here

•Switch plate cap installation completed here

Prior to major component upgrades, downtime typically longer

SNS Major System Downtime Hours by Run Period



Downtime Statistical Data (hours by event)

	Sept.-Dec. 2008	March-July 2009	Sept.-Dec. 2009	Feb.-July 2010	Sept.-Dec. 2010	Σ Hours
Scheduled Beam Hours	3448	3059	2684	3131	2985	15,307
Fault Type						
2/4kV Caps	66	33	25	8	-	132
IGBT	82	43	4	-	-	129
SCR	-	24	8	10	16	58
DFDC Trip	17	26	12	-	-	55
Mod. Tank	5	-	40	-	5	50
Cable Arcing	19	-	5	-	-	24
Rectifier	-	-	-	23	-	23
IGBT Driver	11	5	-	-	6	22
Water Panel	-	9	2	-	1	13
Dif. Voltage	2	5	5	-	-	12
Timing Faults	3	3	3	-	-	9
Oil Pump	-	-	7	-	-	7
Fiber	3	1	-	-	-	4
Misc./?	12	6	70	18	12	118
Σ	220	156	180	59	40	556
Availability	99.54%	99.66%	99.55%	99.87%	99.91%	

Notice: Beam interruption events/hours shown

Downtime Statistical Data (CY-2011)

	2011-1 (Feb. – July)		2011-2 (Sept. - Dec.)		
	Number of events	Hours	Number of events	Hours	Σ Hours
Operational Hours		**3099**		**3353**	**6676**
HV Cable	3	20.3	-	-	20.3
SCR Water Leak (CCL-2)	2	9.2	-	-	9.2
Oil Pump	3	5.2	3	3.3	8.5
IGBT Switch/Driver	3	3.5	2	5.0	8.5
Control chassis (SCL-5, SCL-9)	-	-	2	6.7	6.7
Dynamic Fault (Mod RFQ)	-	-	28	6.2	6.2
Timing Faults	12	2.2	-	-	2.2
Water Panel	1	2.1	-	-	2.1
Voltage Dip (SCL-21)	4	0.5	-	-	0.5
Miscellaneous: Mod. OI, IGBT OI, SCR OI, Flux sat., Dif. V, etc.	Many*	~6	Many*	~2	~8
Σ	28	~49	35	~23	~72
Availability		99.89%		99.95%	
MTTR		1.5		0.6	

*Neutron instrument users are not concerned with minor (<0.5 hour) interruptions but statistics maintained for downtime ≥ 0.1 hour

ESS / SNS Comparison (per modulator basis)

ESS

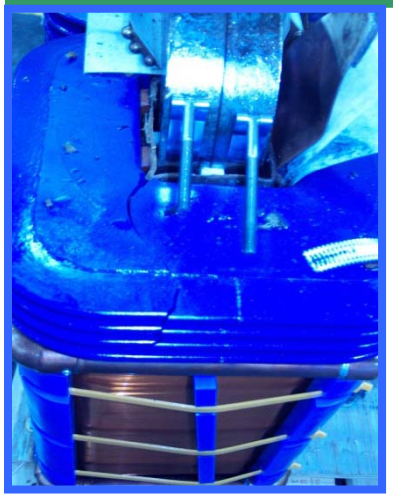
- $MTBF_{goal}$ = 71,000 hr
- $MTTR_{goal}$ = 5 hr
- $A_{goal,all}$ = 99.993%
- A = Σ run hours / (Σ run hours + n×MTTR)
  - n= number of failures during the run period
- 4.6 failures per 6-month (3300 hours used) run period

SNS

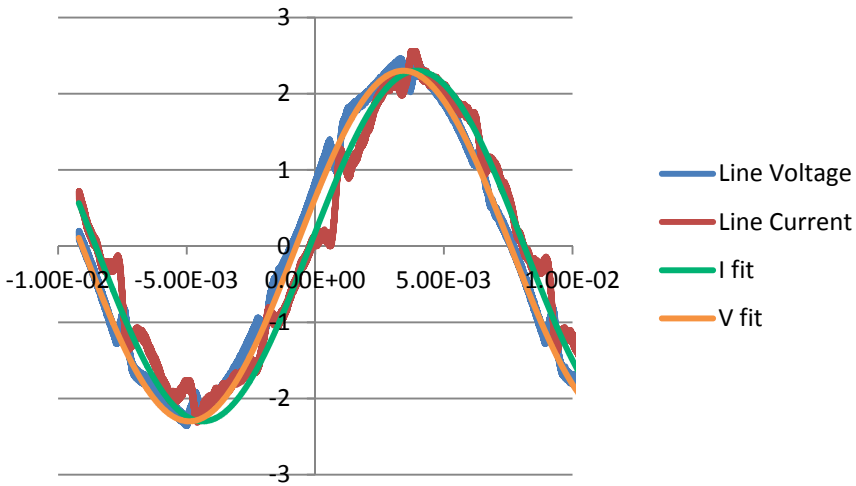
- $MTBF_{goal}$ = 24,000 hr
- $MTTR_{goal}$ = 4 hr
- $A_{goal,all}$ = 99.98%
- $A_{actual,all}$ = 99.92%
- $MTTR_{actual}$ = 1.1 hr
- $MTBF_{actual}$ = MTTR×A/(1-A) ~1500 hr
- Availability only achievable due to much shorter than predicted MTTR w/ “mature” system
- Improvements still needed and under development

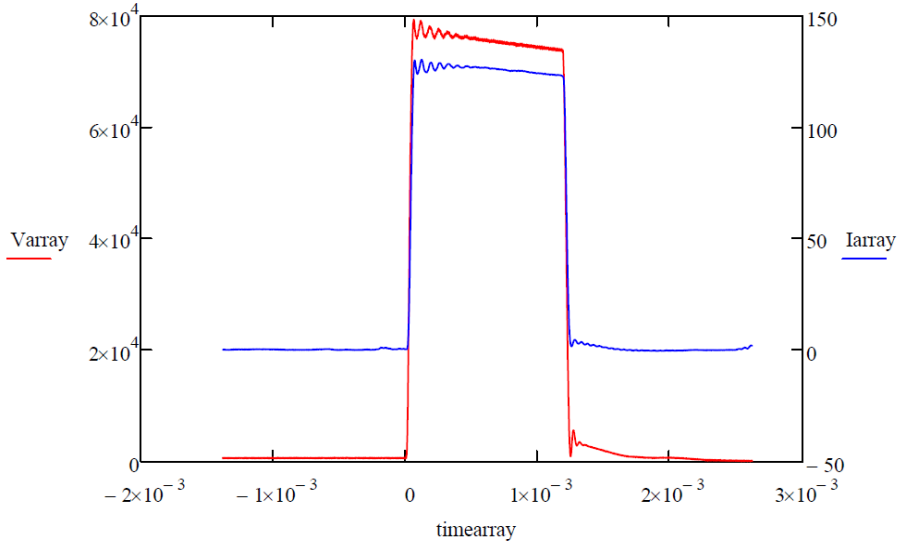
Summary of Major Upgrades To-date

- SCR Controller
  - Snubbers
  - SCR drivers
  - Fast over current protection
  - Forced air cooling
- In-tank components (component derating)
  - Magnetics
  - Capacitors
  - De-Qing resistors
  - Oil distribution / circulation system
- IGBT Switch Plates
  - Optimize pulse length (discussed later)
  - Replace bypass capacitors w/ metallized film
  - Gate drivers (pending)
  - Thorough pre-installation testing
- Reduced SCL klystron loading
- Many others (too numerous to list)



Efficiency – from MathCAD





- Powerouttotal = 60×Energypeak = 6.665×10^5
  - Power output for the entire pulse duration
- PDCout = (PosDCbus + NegDCbus) ×IDCbus = 7.05×10^5
  - Real power delivered to the modulator
- efficiencymod = Powerouttotal / PDCout = 94.5%
- efficiencycalor = Powerouttotal / (Powerouttotal+calorimetrylosses) = 93.3%

- powerSE = 0.5663×flowSE×(TSEexhaust-Tamb) = 1.146×10^4
- powerIGBT = 264×flowIGBT× (TreturnIGBT-Tsupply) = 2.297×10^4
- powerHE = 264×flowHE× (TreturnHE-Tsupply) = 1.309×10^4
- calorimetrylosses = powerSE + powerIGBT + powerHE = 4.752×10^4

- Performance & Past Upgrades
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Controls – Next Generation Controller

The new controller has been designed to address all of the previous controllers shortcomings, speed trouble-shooting & allow for future changes.

CompactRIO systems consists of:

- An embedded controller for communication and processing
- **Reconfigurable** chassis housing the user-programmable FPGA
- Hot-swappable I/O modules
- Graphical LabVIEW software for rapid real-time, Windows, and FPGA programming

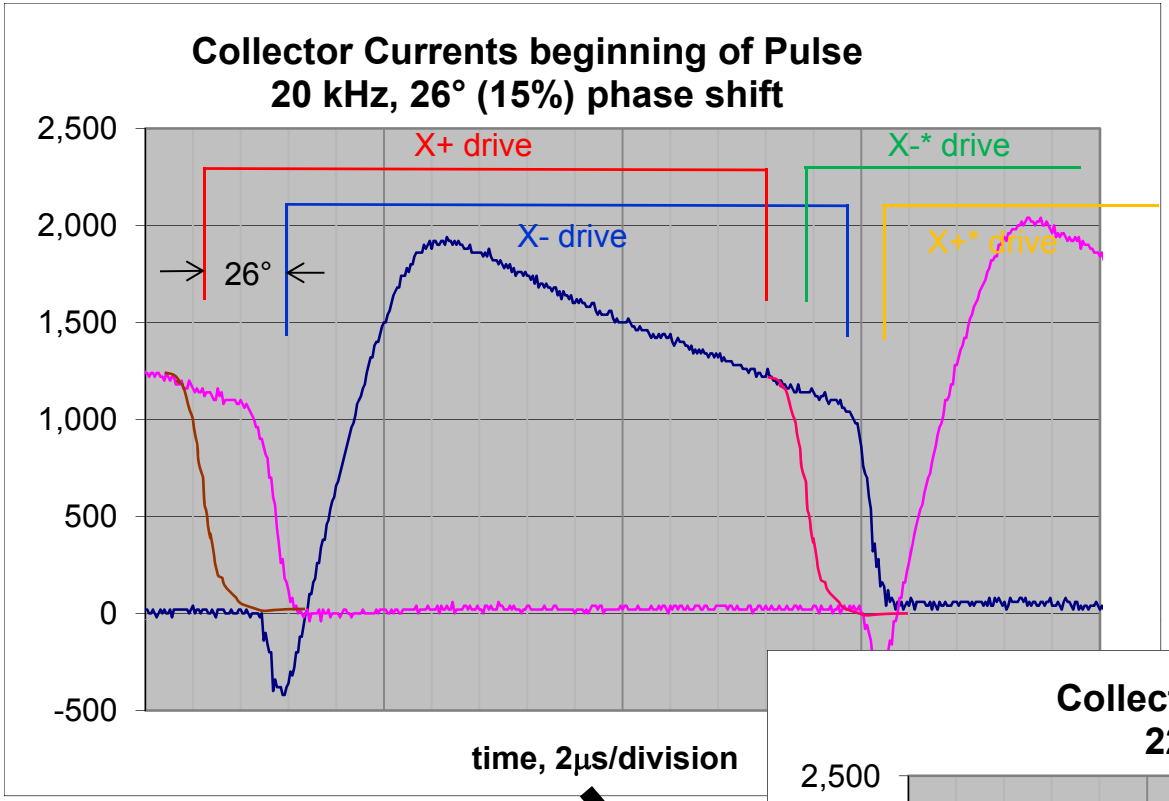
Next Generation Controller

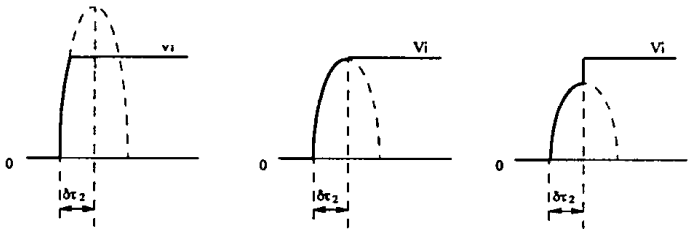
The new controller prototypes provide:

- Waveform capture & data logging, incl. first fault detection
- Flux monitoring, compensation & warnings
- IGBT V_{CE} monitoring & warnings
- Independent IGBT gate control to achieve
  - Variable frequency operation & modulation
  - Phase shifted pulse width modulation
- Complete control of start pulse width, position & phase
- Programmable fault & warning thresholds for all Inputs
- SCR power supply waveform monitoring and warnings
- EPICS interface

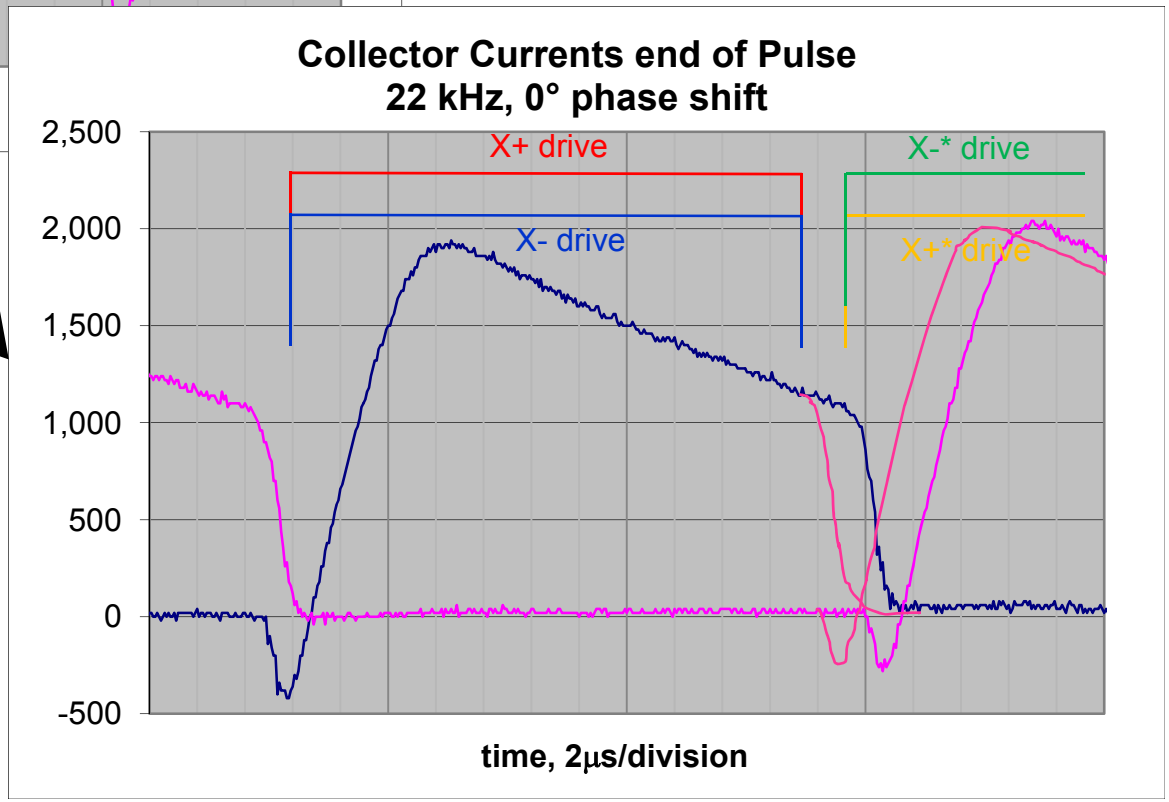
Future versions of the new controller will provide:

- Flexible smoke detector logic
- Control of series switches for IGBT fault isolation
- 3 & 4 phase operation with semi automatic IGBT fault recovery
- IGBT shoot-through monitoring & warnings
- IGBT turn on & turn off monitoring, compensation & warnings



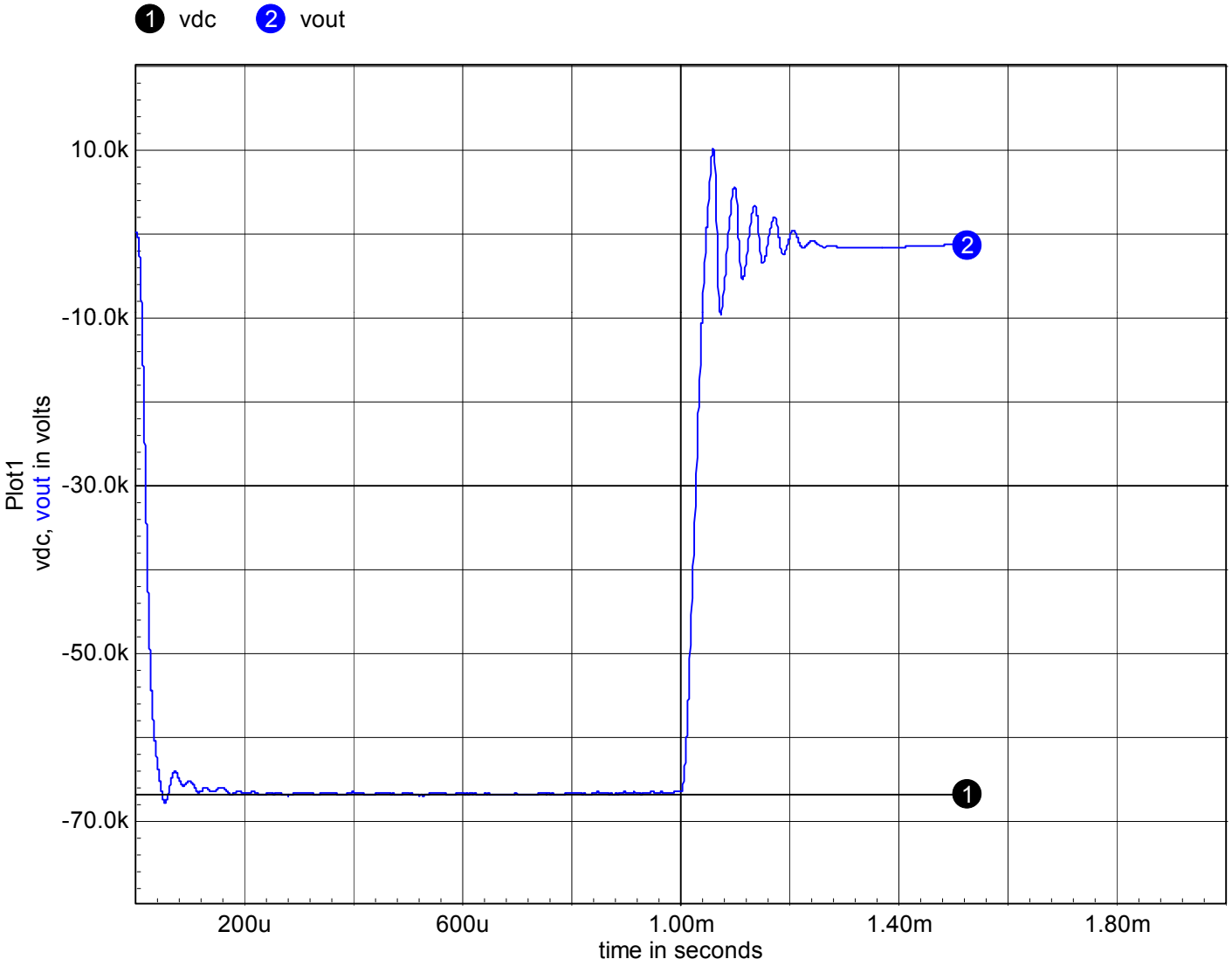


Sabate, et al., Design Considerations for High-Voltage High-Power Full-Bridge Zero-Voltage-Switched PWM Converter, APEC '90, p. 275-284.

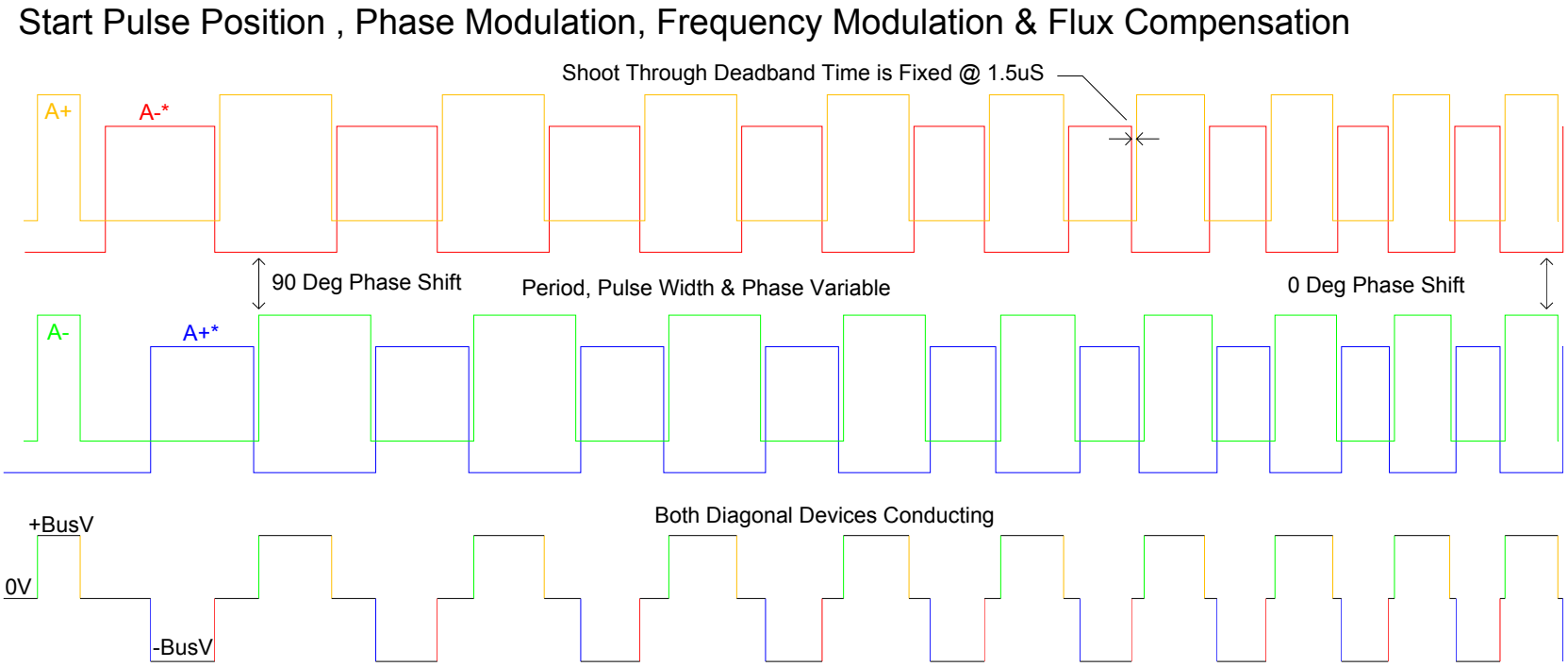


- +/- one diagonal pair, +*/-* other
- Changes "duty cycle" when both diagonal IGBTs conducting
- Maintains almost constant commutation currents throughout macropulse
- Assures ZVS on all IGBT cycles

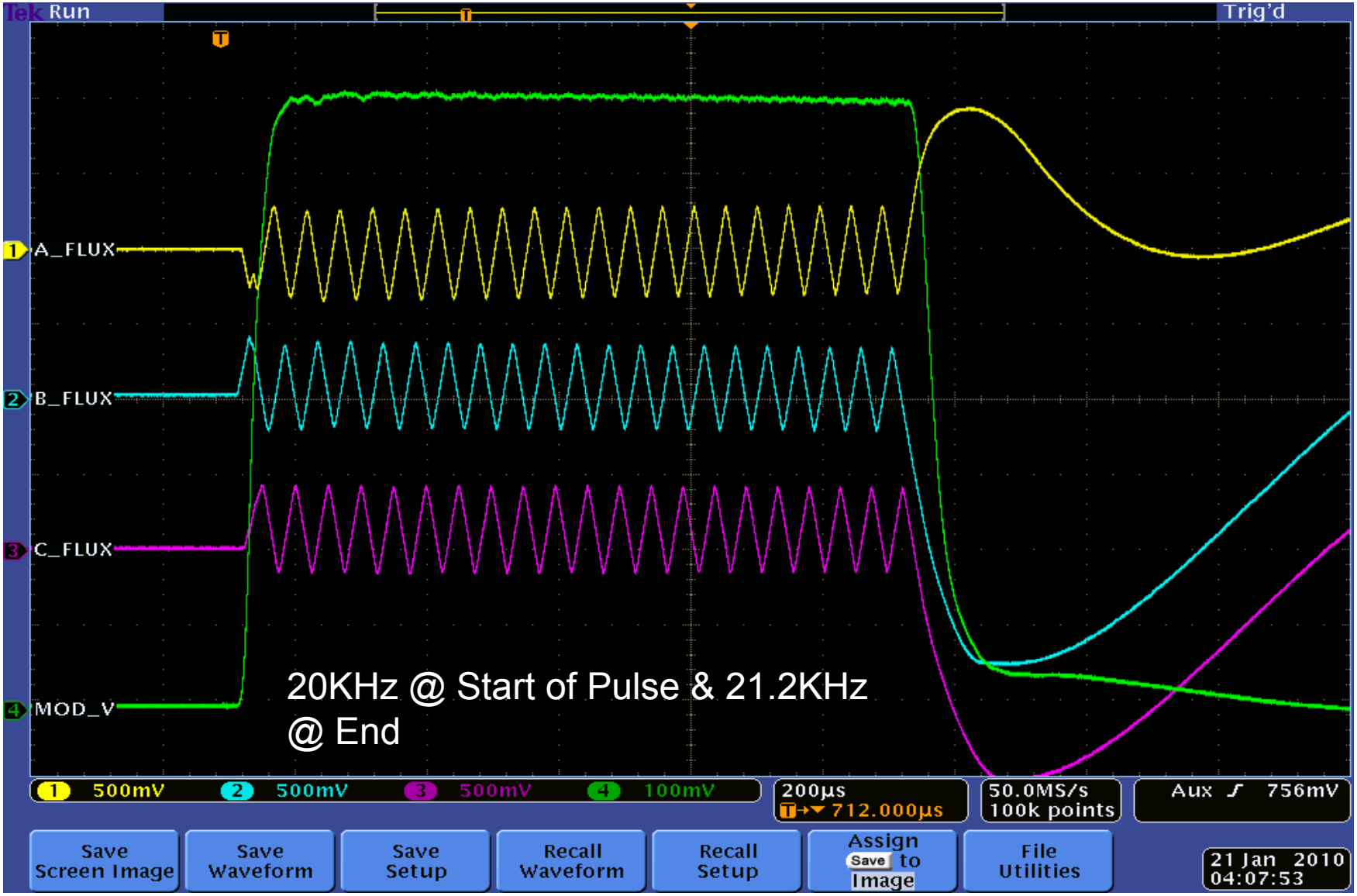
Phase Shift Pulse Width Modulated Output Voltage, 12 klystrons, 1150 V, t=1°/cycle (start pulses not optimized in this simulation



Initial Low-voltage Results with Representative Gate Pulse Signals



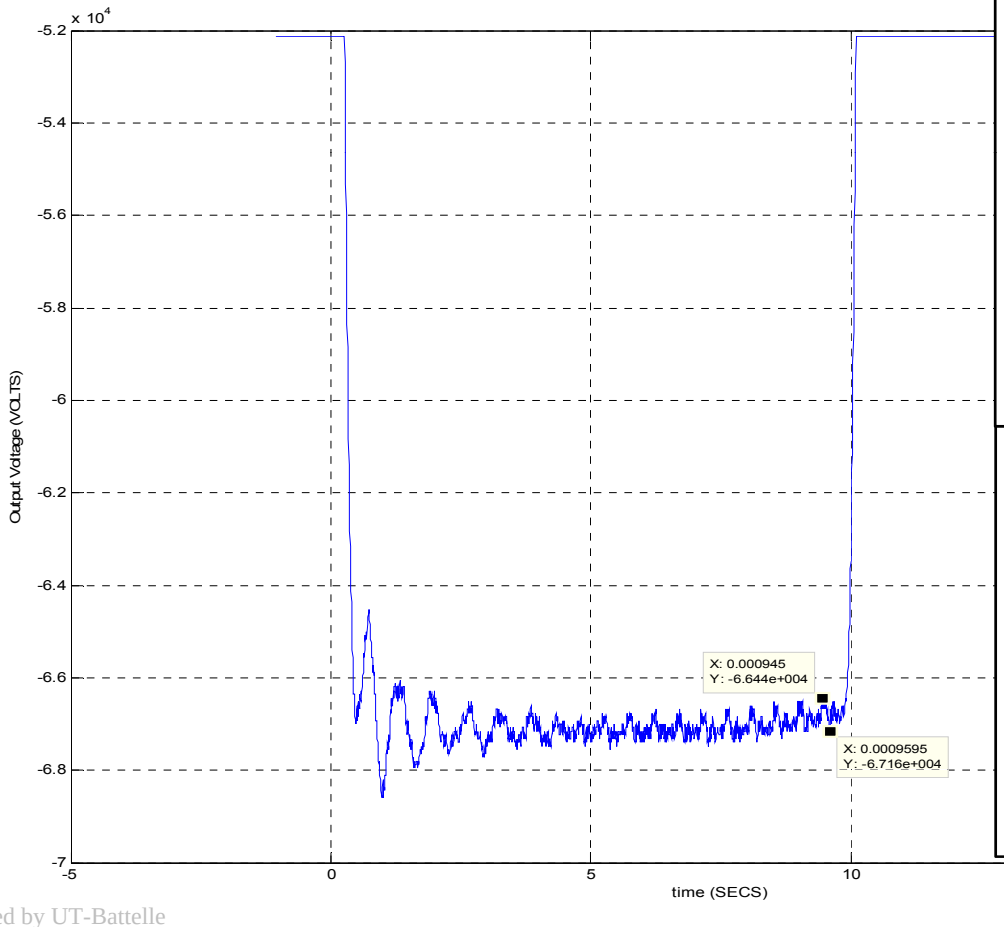
Frequency and Phase Modulation at 400 V Bus

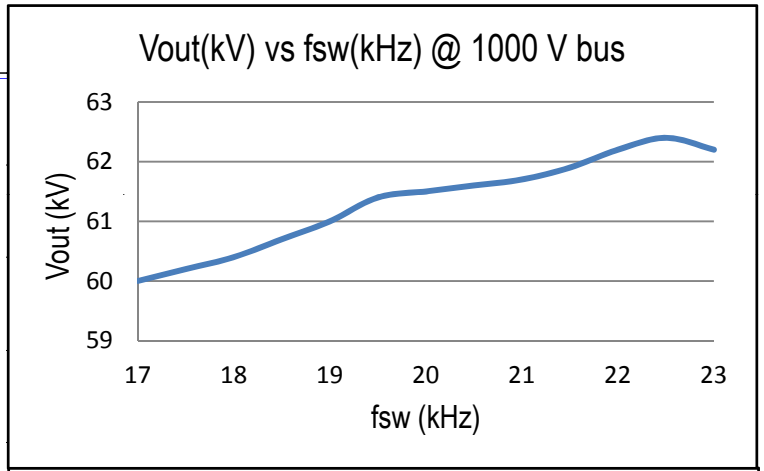


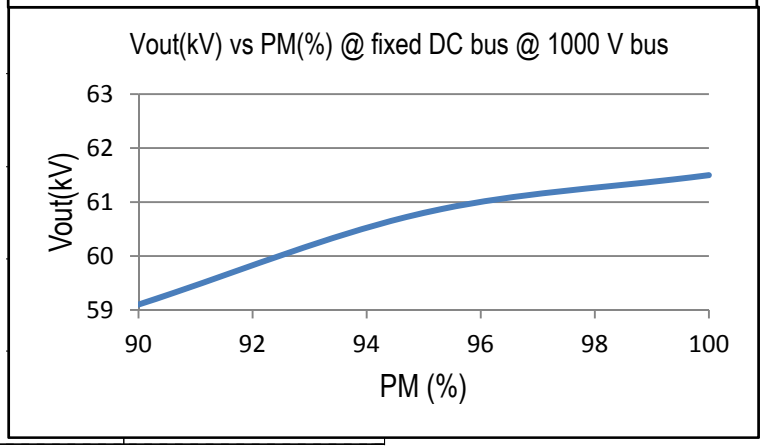
60 Hz Full Power Operation for 1 hour using Phase Shift and Frequency Modulation (start pulses not optimized)

Output Voltage= 61.8 kV
Bus Voltage= +/- 1004 V
FM = 20 kHz to 22 kHz
PSM = 95% to 100%

$\Delta Vdroop$ = 304 V/ms
$\Delta Vripple$ = 664 V





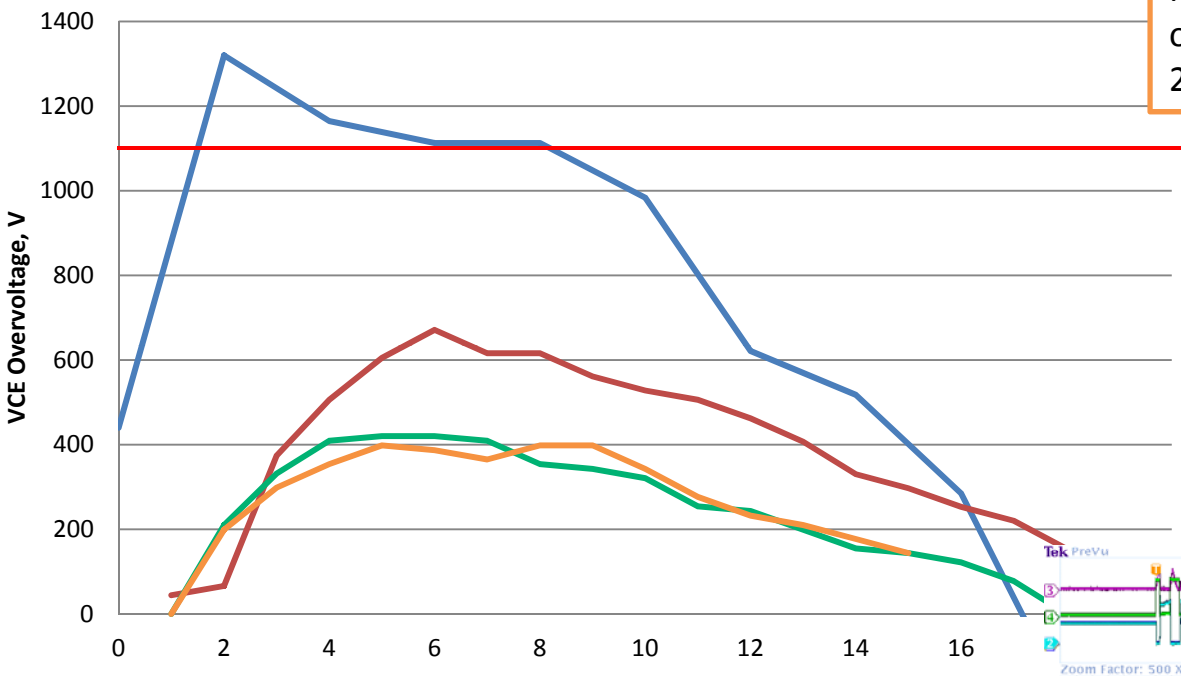


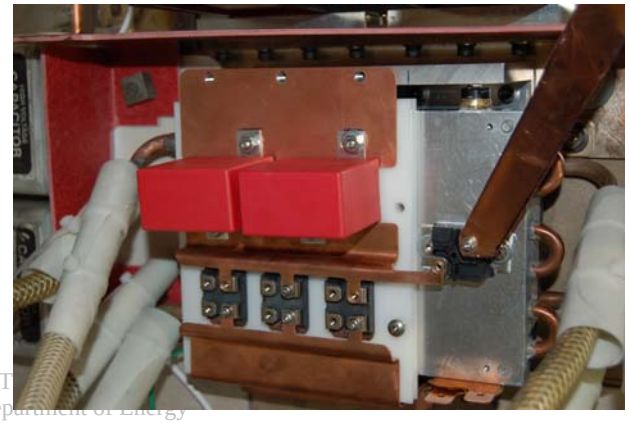
- Performance & Past Upgrades
- UPGRADE – Controls and Alternate IGBT Gating
- UPGRADE – IGBT snubbers
- Alternate topology

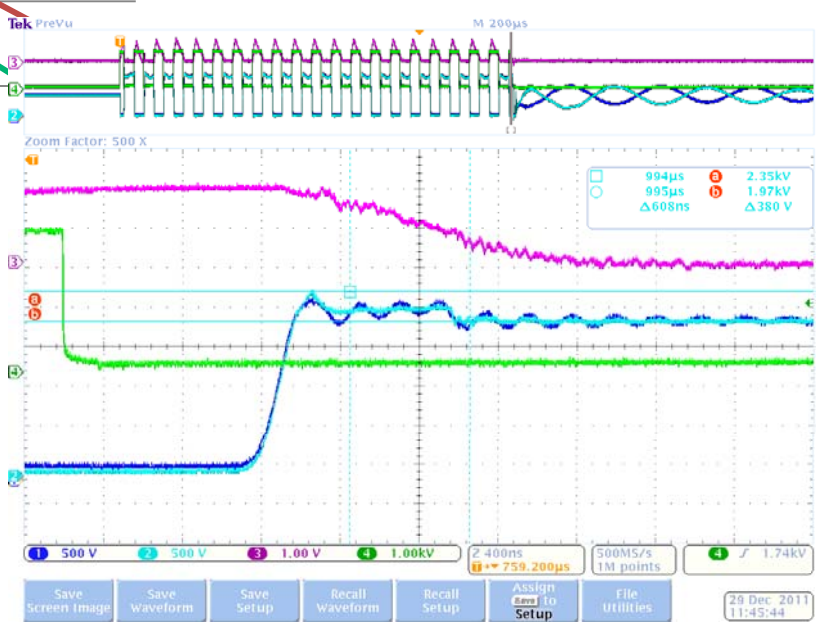
IGBT Snubber – the Problem

End Of Pulse IGBT Over Voltage at +/- 1100 V bus Operation, worst measurable case (to date)

FastHenry simulations reveal bus inductance of ~120 nH, → V= Vbus+Ldi/dt = 2*1100+.120(2200/0.3) = 3100 V







- Performance & Past Upgrades
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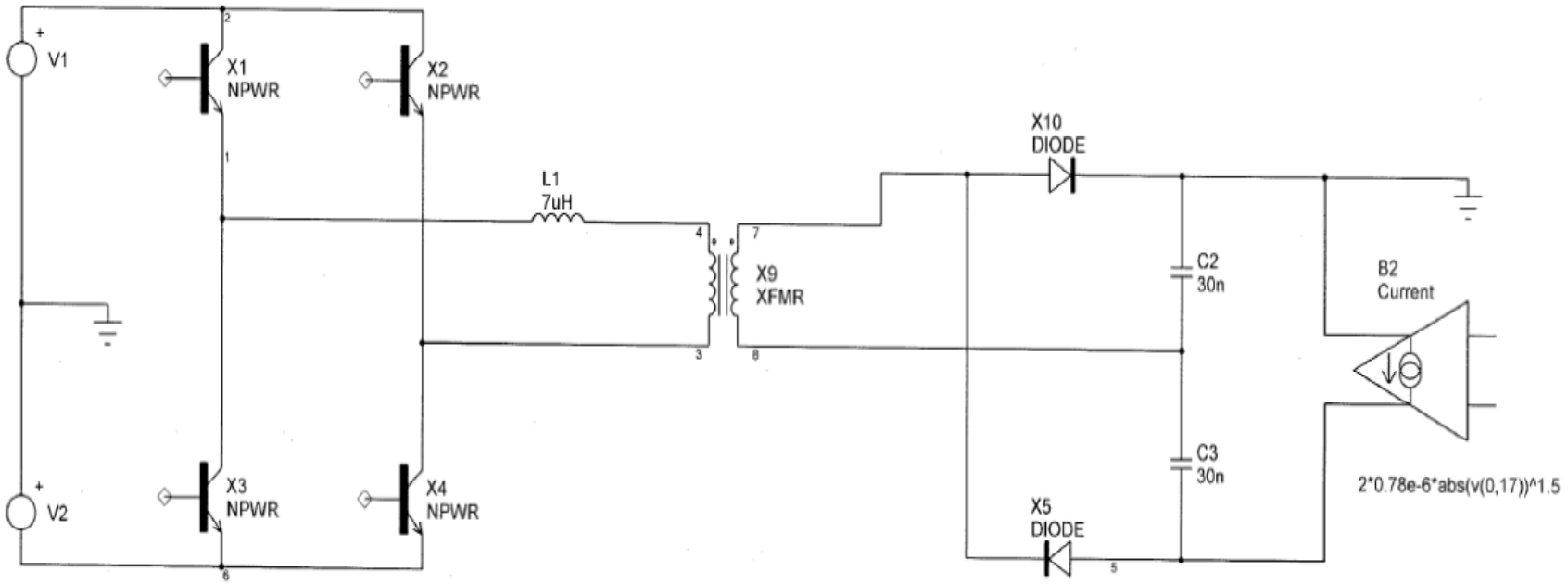
Alternate Topology – modification

Analysis for a NC linac HVCM with 2 DTL 2.5 MW klystrons
Three phases in series. Transformer 13:1 step up ratio



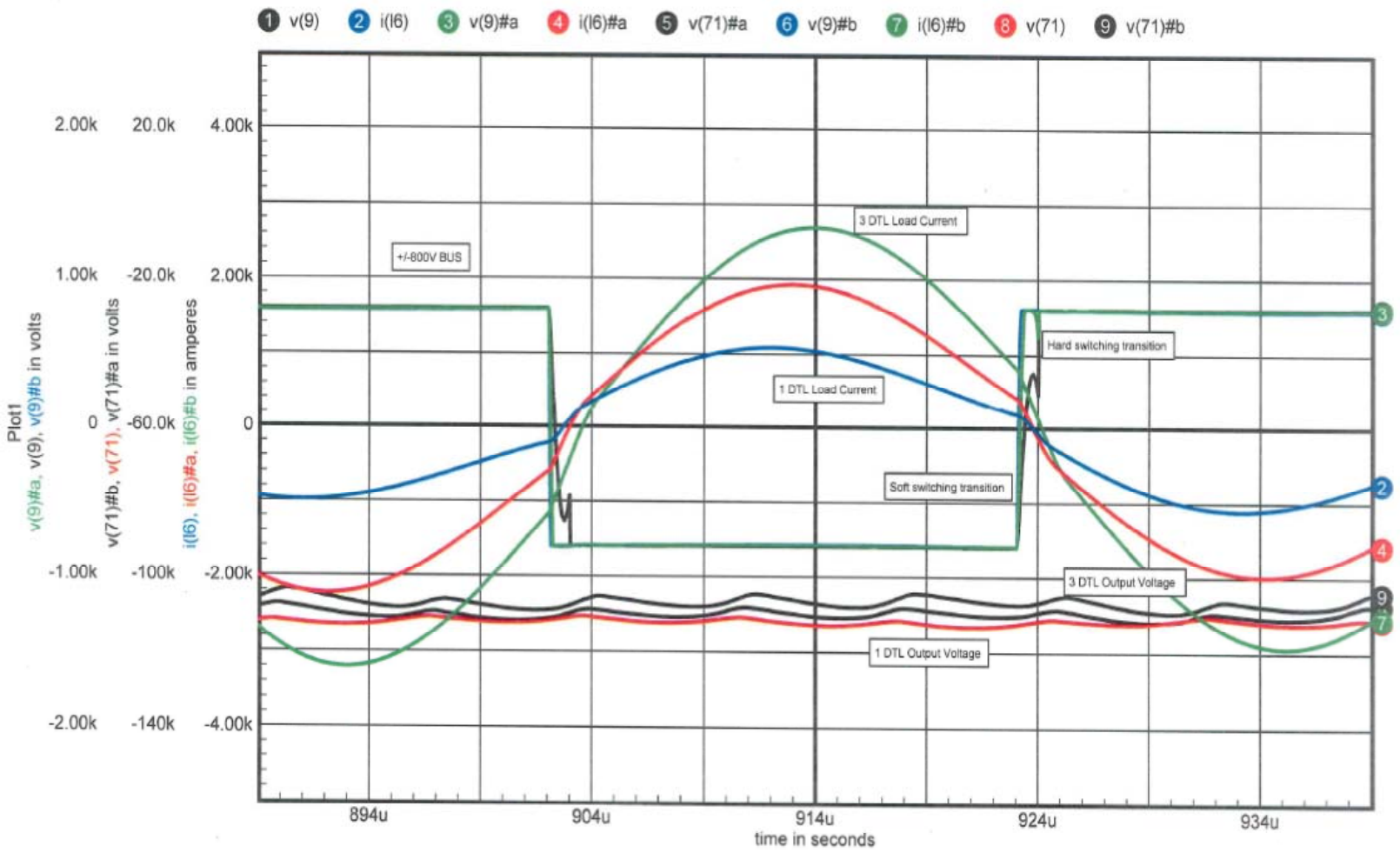
Resonant Period $T_{RES} = 2\pi \sqrt{L_{RES} C_{RES}}$

Characteristic Impedance $Z_C = \sqrt{L_{RES} / C_{RES}}$

Voltage swing across resonant capacitor $\Delta V C_{RES} = I Z_C$

Load change on QRFB

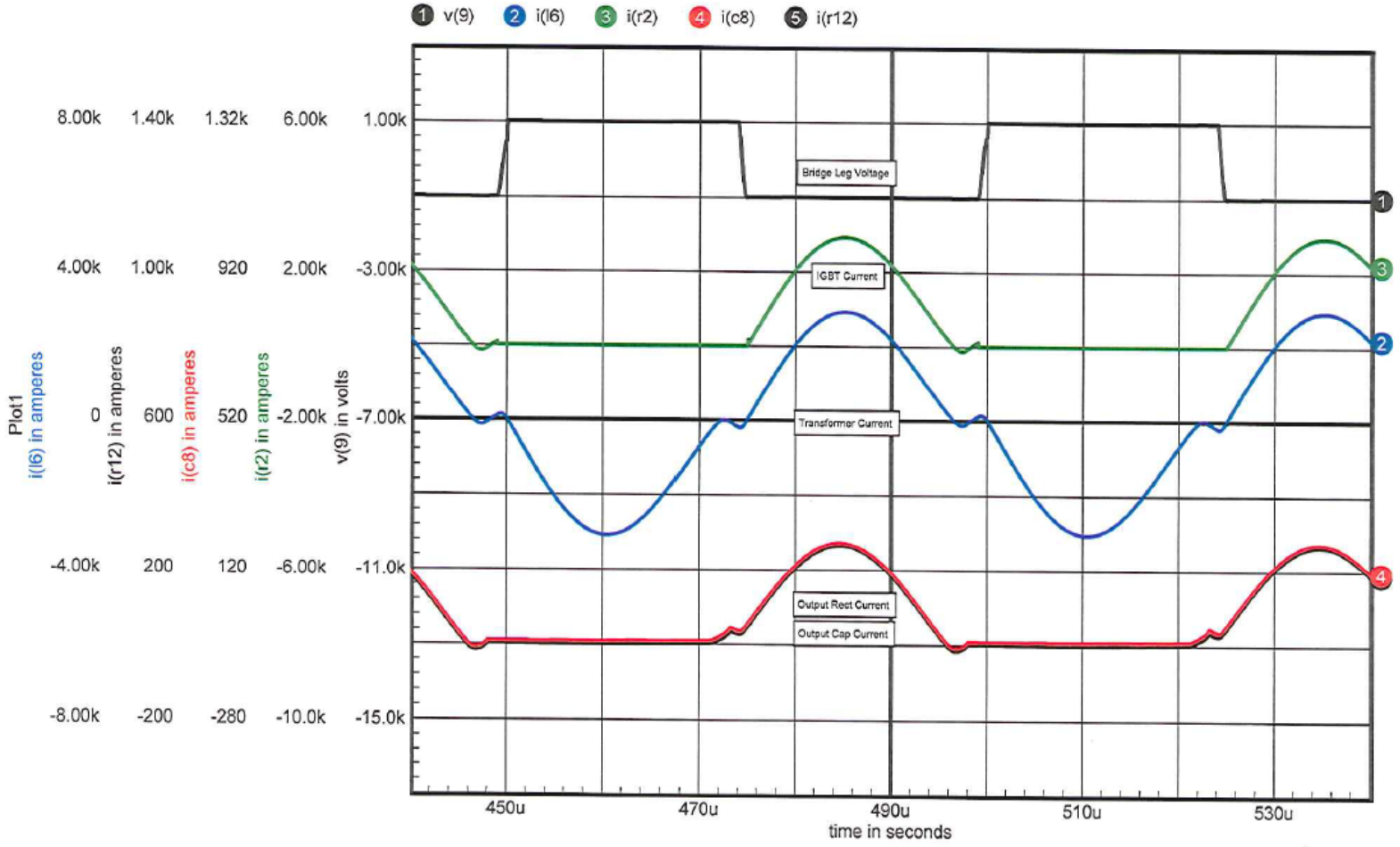
DTL / 2DTL / 3DTL loading comparison



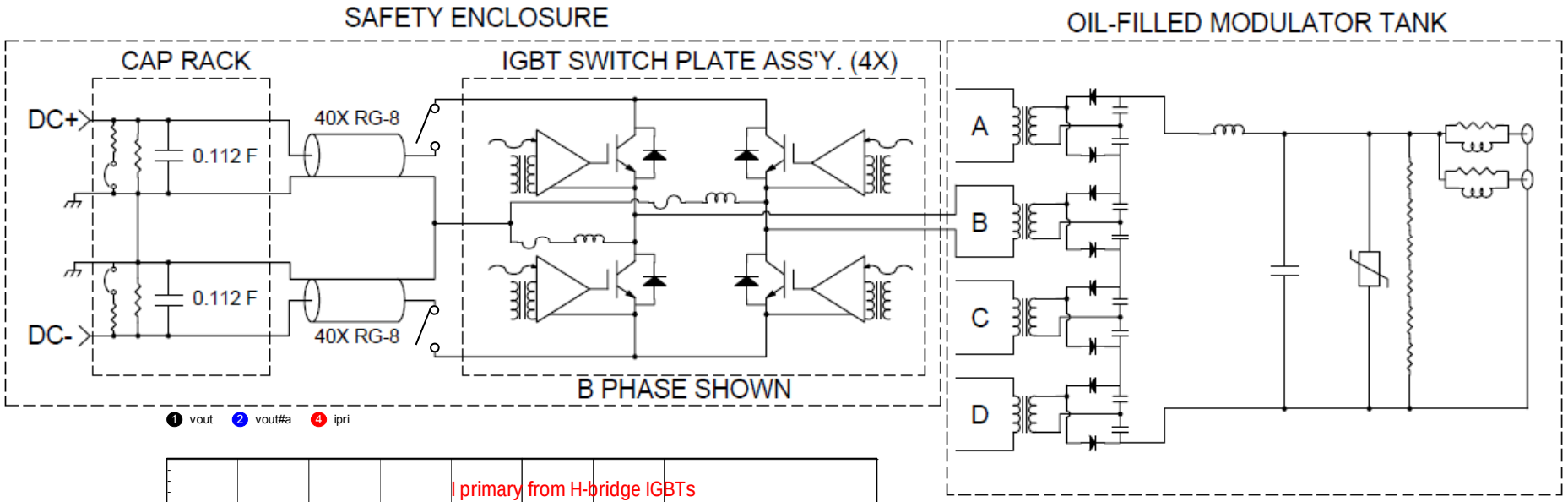
SPICE simulations QRFB topology w/ gapped transformer

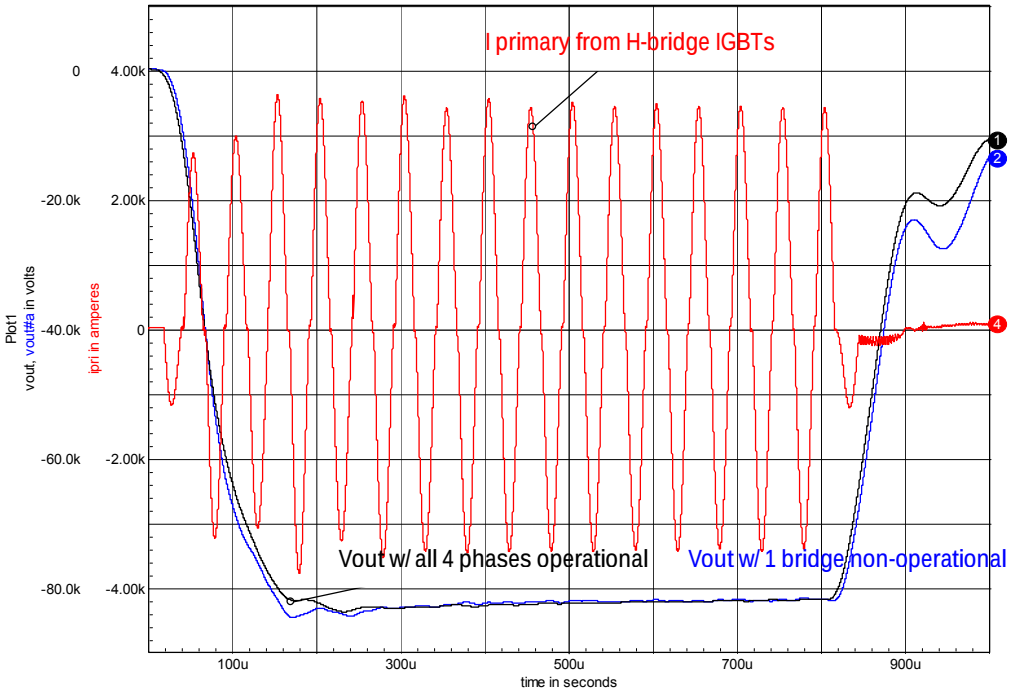
Waveforms for a NC linac HVCM with 2 DTL 2.5 MW klystrons

$$E = \tfrac{1}{2} L_{leak} I^2 = (4/3)\, C_{IGBT}\, V_{in}^2 + \tfrac{1}{2} C_{TR}\, V_{in}^2$$



Series-stacked Redundant System





- 4 phase ► ±750 V DC
- 3 phase ► ±990 V DC
- Timing and circuit values not optimized
- Controller reconfigures system for 3 phase operation

Future Direction in QRFB / alternate topology

- A simple topology modification to reduce stress on IGBTs and output capacitors, extends HVCM flexibility and performance.
- Demonstrated the topology on the test stand in air at 1 MW and ~1% efficiency improvement single phase.
  (1% efficiency gain = 100 kW peak power saving/modulator)
- Resonant capacitors and transformers cores ordered and received.
- Next steps : build new transformers with appropriate turns ratio for > 80kV operation (STS upgrade) and configure for three phase operation in test modulator.

Conclusion

- **HVCM availability improved substantially**

- Synergistic solutions in development to address remaining problems with HVCM to further improve reliability

- Implementation allows for future expansion, major subsystem redundancy

- Parallel investigations of alternate architectures provide even more robust and reliable solutions with minimal perturbations to existing system
  - ORNL interested in developing for 2nd Target Station
  - ESS may want to consider this topology

- **Opportunities for ORNL and ESS to mutually benefit from each other's work & collaborate on development activities**