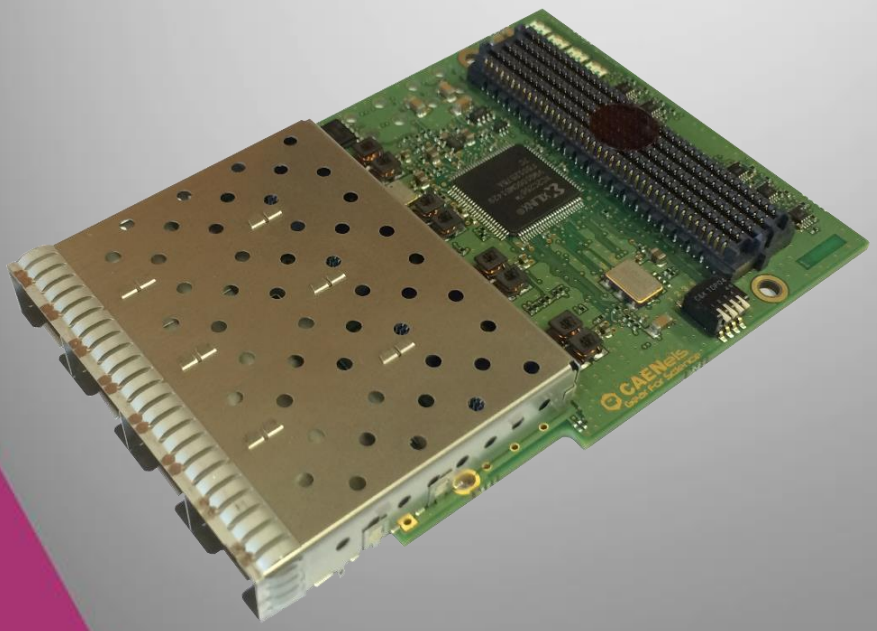
FMC-4SFP+

Dual- and Quad-channel SFP/SFP+ FMC Adapter

CAENels
Gear for Science

Pin Assignments



FMC - FPGA MEZZANINE CARD

Rev. 1.1 – April 2016

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Document Revisions

Document Revision	Date	Comment
1.0	November 5th 2015	First Release
1.1	April 1st 2016	Corrected VADJ range

Safety information - Warnings

CAEN ELS will repair or replace any product within the guarantee period if the Guarantor declares that the product is defective due to workmanship or materials and has not been caused by mishandling, negligence on behalf of the User, accident or any abnormal conditions or operations.

Please read carefully the manual before operating any part of the instrument

WARNING

Do NOT open the boxes

CAEN ELS d.o.o. declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly this User's Manual before any kind of operation.

CAEN ELS d.o.o. reserves the right to change partially or entirely the contents of this Manual at any time and without giving any notice.

Disposal of the Product

The product must never be dumped in the Municipal Waste. Please check your local regulations for disposal of electronics products.

Read over the instruction manual carefully before using the instrument.
The following precautions should be strictly observed before using the device:

WARNING

- Do not use this product in any manner not specified by the manufacturer. The protective features of this product may be impaired if it is used in a manner not specified in this manual.
- Do not use the device if it is damaged. Before you use the device, inspect the instrument for possible cracks or breaks before each use.
- Do not operate the device around explosives gas, vapor or dust.
- Always use the device with the cables provided.
- Turn off the device before establishing any connection.
- Do not operate the device with the cover removed or loosened.
- Do not install substitute parts or perform any unauthorized modification to the product.
- Return the product to the manufacturer for service and repair to ensure that safety features are maintained

CAUTION

- This instrument is designed for indoor use and in area with low condensation.

The following table shows the general environmental requirements for a correct operation of the instrument:

Environmental Conditions	Requirements
Operating Temperature	0°C to 50°C
Operating Humidity	30% to 85% RH (non-condensing)
Storage Temperature	-10°C to 60°C
Storage Humidity	5% to 90% RH (non-condensing)

1. Introduction

This chapter describes the general characteristics and main features of the CAEN ELS FMC-SFP mezzanine cards.

1.1 FMC-SFP Overview

The CAEN ELS FMC-SFP is a standard FPGA Mezzanine Card (FMC) Low Pin Count (LPC) daughter board that allows to communicate up to 4 high speed hot-swappable SFP+ devices. The board is available in two different versions:

- **FMC-4SFP+** version: with 4 fast SFP/SFP+ channels, without front panel;
- **FMC-2SFP+** version: with 2 fast SFP/SFP+ channels, with standard FMC bezel.

The board is electrically compliant to the FMC standard (ANSI/VITA 57.1). All module pins are translated to the FMC carrier voltage VADJ that can be in the range from 1.5V to 3.3V. With its low operation voltage it can be used on almost all carriers. The module is compatible with LPC and HPC carrier boards.

The components are placed to be compatible also with carriers that have components under the FMC module. The SFP+ cages are placed to fi all carriers without front panel modifications.

The module mounts an oscillator chip that can be configured using the I2C-controlled LVDS (Low Voltage Differential Signaling) interface. The start-up frequency could be also decided using a DIP switch present on the board (Autonomous Mode). The operating frequency range of the chis is from 10 MHz up to 280 MHz.

1.2 FMC connections

In the following sections are described all the FMC connection with the FMC-SFP board.

1.2.1 ROW A

All FMC ROW A GND pins are connected to ground and are not listed in the following table.

Pin #	Pin Name	Connectivity	IO Standard	Remark
A2	DP1_M2C_P	Module 2 RX (inner module)	module dependent, SFF-8418	FMC output
A3	DP1_M2C_N	Module 2 RX (inner module)	module dependent, SFF-8418	FMC output
A6	DP2_M2C_P	Module 4 RX (outer module)	module dependent, SFF-8418	FMC output (*)
A7	DP2_M2C_N	Module 4 RX (outer module)	module dependent, SFF-8418	FMC output (*)
A10	DP3_M2C_P	Module 1 RX (outer module)	module dependent, SFF-8418	FMC output (*)
A11	DP3_M2C_N	Module 1 RX (outer module)	module dependent, SFF-8418	FMC output (*)
A14	DP3_M2C_P	Not Connected	/	/
A15	DP3_M2C_N	Not Connected	/	/
A18	DP3_M2C_P	Not Connected	/	/
A19	DP3_M2C_N	Not Connected	/	/
A22	DP1_C2M_P	Module 2 TX (inner module)	module dependent, SFF-8418	FMC input
A23	DP1_C2M_N	Module 2 TX (inner module)	module dependent, SFF-8418	FMC input
A26	DP2_C2M_P	Module 4 TX (outer module)	module dependent, SFF-8418	FMC input (*)
A27	DP2_C2M_N	Module 4 TX (outer module)	module dependent, SFF-8418	FMC input (*)
A30	DP3_C2M_P	Module 1 TX (outer module)	module dependent, SFF-8418	FMC input (*)
A31	DP3_C2M_N	Module 1 TX (outer module)	module dependent, SFF-8418	FMC input (*)
A34	DP3_C2M_P	Not Connected	/	/
A35	DP3_C2M_N	Not Connected	/	/
A38	DP3_C2M_P	Not Connected	/	/
A39	DP3_C2M_N	Not Connected	/	/

Table 1: FMC Row A connections; (*) available only in 4-channel version

1.2.1 ROW B

All FMC ROW B GND pins are connected to ground and the other pins are left unconnected.

1.2.1 ROW C

All FMC ROW C GND pins are connected to ground and are not listed in the following table.

Pin #	Pin Name	Connectivity	IO Standard	Remark
C2	DP0_C2M_P	Module 3 TX (inner module)	module dependent, SFF-8418	FMC input
C3	DP0_C2M_N	Module 3 TX (inner module)	module dependent, SFF-8418	FMC input
C6	DP0_M2C_P	Module 3 RX (inner module)	module dependent, SFF-8418	FMC output
C7	DP0_M2C_N	Module 3 RX (inner module)	module dependent, SFF-8418	FMC output
C10	LA06_P	MODABS Module 4	LVCMOS (VADJ)	FMC output (*)
C11	LA06_N	MODABS Module 3	LVCMOS (VADJ)	FMC output (*)
C14	LA10_P	RS0 Module 4	LVCMOS (VADJ)	FMC input (*)
C15	LA10_N	RS0 Module 3	LVCMOS (VADJ)	FMC input (*)
C18	LA14_P	Reserved	LVCMOS (VADJ)	Do not use
C19	LA14_N	Reserved	LVCMOS (VADJ)	Do not use
C22	LA18_CC_P	Reserved	LVCMOS (VADJ)	Do not use
C23	LA18_CC_N	Reserved	LVCMOS (VADJ)	Do not use
C26	LA27_P	Not Connected	/	/
C27	LA27_N	Not Connected	/	/
C30	SCL_C	EEPROM SCL	LVCMOS (+3V3PAUX)	/
C31	SDA_C	EEPROM SDA	LVCMOS (+3V3PAUX)	/
C34	GA0	EEPROM GA0	LVCMOS (+3V3PAUX)	/
C35	+12V	Not Connected	/	/
C38	+12V	Not Connected	/	/
C39	+3V3	Board Power Supply	/	/

Table 2: FMC Row C connections; (*) available only in 4-channel version

1.2.1 ROW D

All FMC ROW D GND pins are connected to ground and are not listed in the following table.

Pin #	Pin Name	Connectivity	IO Standard	Remark
D1	PG_C2M	Connected to on-board logic	/	Do not use
D4	GBTCLK0_M2C_P	Si570 Oscillator Output	LVDS	Frequency according to dip switches (see Chapter 2)
D5	GBTCLK0_M2C_N	Si570 Oscillator Output	LVDS	Frequency according to dip switches (see Chapter 2)
D8	LA01_CC_P	Reserved	LVCMOS (VADJ)	Do not use
D9	LA01_CC_N	Reserved	LVCMOS (VADJ)	Do not use
D11	LA05_P	RXLOS Module 2	LVCMOS (VADJ)	FMC output
D12	LA05_N	RXLOS Module 1	LVCMOS (VADJ)	FMC output
D14	LA09_P	TXDISABLE Module 2	LVCMOS (VADJ)	FMC input
D15	LA09_N	TXDISABLE Module 1	LVCMOS (VADJ)	FMC input
D17	LA13_P	RS1 Module 2	LVCMOS (VADJ)	FMC input
D18	LA13_N	RS1 Module 1	LVCMOS (VADJ)	FMC input
D20	LA17_CC_P	Reserved	LVCMOS (VADJ)	Do not use
D21	LA17_CC_N	Reserved	LVCMOS (VADJ)	Do not use
D23	LA23_P	I2C SCL Module 4	LVCMOS (VADJ) open drain	I2C (*)
D24	LA23_N	I2C SDA Module 4	LVCMOS (VADJ) open drain	I2C (*)
D26	LA26_P	Not Connected	/	/
D27	LA26_N	Not Connected	/	/
D29	TCK	Connected to on-board logic	LVCMOS (3.3V)	Do not use
D30	TDI	Connected to on-board logic	LVCMOS (3.3V)	Do not use
D31	TDO	Connected to on-board logic	LVCMOS (3.3V)	Do not use
D32	+3V3AUX	EEPROM +3.3V AUX	/	/
D33	TMS	Connected to on-board logic	LVCMOS (3.3V)	Do not use
D34	TRST_L	Not Connected	/	/

Pin #	Pin Name	Connectivity	IO Standard	Remark
D35	GA1	EEPROM GA1	LVCMOS (+3V3PAUX)	/
D36	+3V3	Board Power Supply	/	/
D38	+3V3	Board Power Supply	/	/
D40	+3V3	Board Power Supply	/	/

Table 3: FMC Row D connections; (*) available only in 4-channel version

1.2.1 ROW E

All FMC ROW E GND pins are connected to ground and the other pins are left unconnected, except the PIN E39 (see the following table).

Pin #	Pin Name	Connectivity	IO Standard	Remark
E39	VADJ	IO Pins Power Supply	/	Not used in LPC carriers

Table 4: FMC Row E connection

1.2.1 ROW F

All FMC ROW F GND pins are connected to ground and the other pins are left unconnected, except the PIN F40 (see the following table).

Pin #	Pin Name	Connectivity	IO Standard	Remark
F40	VADJ	IO Pins Power Supply	/	Not used in LPC carriers

Table 5: FMC Row F connection

1.2.1 ROW G

All FMC ROW G GND pins are connected to ground and are not listed in the following table.

Pin #	Pin Name	Connectivity	IO Standard	Remark
G2	CLK0_C2M_P	Not Connected	/	/
G3	CLK0_C2M_N	Not Connected	/	/
G6	LA00_CC_P	Reserved	LVCMOS (VADJ)	Do not use

Pin #	Pin Name	Connectivity	IO Standard	Remark
G7	LA00_CC_N	Reserved	LVCMOS (VADJ)	Do not use
G9	LA03_P	TXFAULT Module 2	LVCMOS (VADJ)	FMC output
G10	LA03_N	TXFAULT Module 1	LVCMOS (VADJ)	FMC output
G12	LA08_P	TXDISABLE Module 4	LVCMOS (VADJ)	FMC input (*)
G13	LA08_N	TXDISABLE Module 3	LVCMOS (VADJ)	FMC input (*)
G15	LA12_P	RS1 Module 4	LVCMOS (VADJ)	FMC input (*)
G16	LA12_N	RS1 Module 3	LVCMOS (VADJ)	FMC input (*)
G18	LA16_P	Reserved	LVCMOS (VADJ)	Do not use
G19	LA16_N	Reserved	LVCMOS (VADJ)	Do not use
G21	LA20_P	Not Connected	/	/
G22	LA20_N	Not Connected	/	/
G24	LA22_P	I2C SCL Module 2	LVCMOS (VADJ) open drain	I2C
G25	LA22_N	I2C SDA Module 2	LVCMOS (VADJ) open drain	I2C
G27	LA25_P	Si570 Oscillator I2C SCL	LVCMOS (VADJ) open drain	Programmed after reset regarding DIP Sw.
G28	LA25_N	Si570 Oscillator I2C SDA	LVCMOS (VADJ) open drain	Programmed after reset regarding DIP Sw.
G30	LA29_P	Not Connected	/	/
G31	LA29_N	Not Connected	/	/
G33	LA31_P	Not Connected	/	/
G34	LA31_N	Not Connected	/	/
G36	LA33_P	Not Connected	/	/
G37	LA33_N	Not Connected	/	/
G39	VADJ	IO Pins Power Supply	/	/

Table 6: FMC Row G connections; (*) available only in 4-channel version

1.2.1 ROW H

All FMC ROW H GND pins are connected to ground and are not listed in the following table.

Pin #	Pin Name	Connectivity	IO Standard	Remark
H1	VREF_A_M2C	Not Connected	/	/

Pin #	Pin Name	Connectivity	IO Standard	Remark
H2	PRSNT_M2C#	GND	/	/
H4	CLK0_M2C_P	Not Connected	/	/
H5	CLK0_M2C_N	Not Connected	/	/
H7	LA02_P	TXFAULT Module 4	LVCMOS (VADJ)	FMC output (*)
H8	LA02_N	TXFAULT Module 3	LVCMOS (VADJ)	FMC output (*)
H10	LA04_P	RXLOS Module 4	LVCMOS (VADJ)	FMC output (*)
H11	LA04_N	RXLOS Module 3	LVCMOS (VADJ)	FMC output (*)
H13	LA07_P	MODABS Module 2	LVCMOS (VADJ)	FMC output
H14	LA07_N	MODABS Module 1	LVCMOS (VADJ)	FMC output
H16	LA11_P	RS0 Module 2	LVCMOS (VADJ)	FMC input
H17	LA11_N	RS0 Module 1	LVCMOS (VADJ)	FMC input
H19	LA15_P	Reserved	LVCMOS (VADJ)	Do not use
H20	LA15_N	Reserved	LVCMOS (VADJ)	Do not use
H22	LA19_P	Reserved	LVCMOS (VADJ)	Do not use
H23	LA19_N	Reserved	LVCMOS (VADJ)	Do not use
H25	LA21_P	I2C SCL Module 1	LVCMOS (VADJ) open drain	I2C
H26	LA21_N	I2C SDA Module 1	LVCMOS (VADJ) open drain	I2C
H28	LA24_P	I2C SCL Module 3	LVCMOS (VADJ) open drain	I2C (*)
H29	LA24_N	I2C SDA Module 3	LVCMOS (VADJ) open drain	I2C (*)
H31	LA28_P	Not Connected	/	/
H32	LA28_N	Not Connected	/	/
H34	LA30_P	Not Connected	/	/
H35	LA30_N	Not Connected	/	/
H37	LA32_P	Not Connected	/	/
H38	LA32_N	Not Connected	/	/
H40	VADJ	IO Pins Power Supply	/	/

Table 7: FMC Row H connections; (*) available only in 4-channel version

1.2.1 ROW J

All FMC ROW J GND pins are connected to ground and the other pins are left unconnected.

1.2.1 ROW K

All FMC ROW K GND pins are connected to ground and the other pins are left unconnected.

2. Clock Generation

The CAEN ELS FMC-SFP mounts also a Clock Generator Chip Silicon ***Labs SI570*** (570BBC000121DG), which allows to generate random low-jitter clock at any frequency ranging from 10 MHz to 280 MHz.

At power-up of the board, the SI570 chip generates a frequency according to the configuration of DIP Switches. In the following table are summarized the possible start-up DIP switches configurations:

Switch #3	Switch #2	Switch #1	Clock Frequency
0	0	0	125.00 MHz
0	0	1	156.25 MHz
0	1	0	162.50 MHz
0	1	1	178.25 MHz
1	0	0	200.00 MHz
1	0	1	203.15 MHz
1	1	0	250.00 MHz
1	1	1	Do not use

Table 8: Start-up Clock Frequency

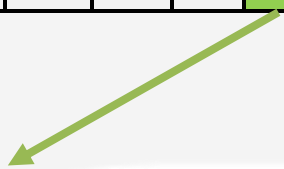
The Silicon Labs clock generation chip is accessible also using the I2C bus, so it is possible to communicate directly with the chip to configure it and to generate the desired clock frequency. The I2C interface is accessible using the pins: LA25_P (Si570 I2C SCL) and LA25_N (Si570 I2C SDA). For additional information regarding the Si570 please refer to its datasheet.

The DIP Switch #4 determinates the mode of operation. When it is set to 1, all pins have to be controlled by the Carrier Board. If there is not an interaction with the board, then the FMC-SFP will not generate a clock. Otherwise, when this switch is set to 1, the module is enabled and the communication with the Carrier Board is disabled.

3. Ordering Options

The **FMC-SFP+** board is available in two main different versions:

F	M	C	-	X	S	F	P



4	**FMC-4SFP+** version: with 4 fast SFP/SFP+ channels, without front panel (ordering code: FMC4SFP4XAAA)
2	**FMC-2SFP+** version: with 2 fast SFP/SFP+ channels, with standard FMC bazel (ordering code: FMC4SFP2XAAA)

NOTE: *fields/characters shaded in grey color are fixed.*

Table 9: Ordering Options

4. Technical Specifications

Technical Specifications of the FMC-SFP+ boards are herein presented.

Technical Specification	FMC-SFP+
Board Type	FPGA Mezzanine Card - FMC VITA 57.1
FMC Connector Type	LPC (HPC compliant)
Number of SFP+ Channels	2 on FMC-2SFP+ 4 on FMC-4SFP+
VADJ Range	1.5 V – 3.3 V
On-board Oscillator Range	10 MHz – 280 MHz
On-board Oscillator Configuration Protocol	I2C
Other Features	Link Status indication via front panel or bottom-emitting LEDs Autonomous Mode: Clock speed setting and transmitter activation via DIP switches

Table 10: Technical Specifications