IFC_1410 & IFC_1420
MTCA.4 Single Board Computers
Overview

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Disclaimer

This document presents an overview of the IFC_1410, IFC_1420 and RXI_1460 boards as defined in the corresponding Conceptual Design documents. The actual design of these board is subject to discussion. Please consult the Open Issues documents.

Plan

- Introduction
- Roadmap
- Side-by-side comparison IFC_1210 vs IFC_1410
- IFC_1410 Architecture
- IFC_1420 Architecture
- Rear Transition Module (RXI_1460)
- Conclusion

Introduction

- The IFC_1410 is an evolution of the IFC_1210
- It supports the same eco-system :
  - FMC products (DACs & ADCs)
  - Tosca FPGA Design Kit
  - Software products (Linux-based)
- The IFC_1420 is a variant of the IFC_1410 with an on-board ADC function
- The differences between the IFC_1410 and IFC_1210 are given hereafter

Roadmap

IOxOS Commitment to the MTCA.4 Form Factor

Front-Side Boards

- IFC_1410 : Intelligent FMC Carrier
- *IFC_1411 : Hypothetical next generation of IFC*
- IFC_1420 : IFC_1410 + ADC3110/3111
- *IFC_1421 : Hypothetical variant/evolution of IFC_1420*

Rear-Side Boards

- RXI_1460 : XMC/PMC and IO extension for IFC_1410
- *RXI_1461 : Hypothetical FMC carrier*
- *RCE_1470 : Hypothetical COM Express processing board*

Side-by-side Comparison
IFC_1210 vs IFC_1410

Form-Factor

Feature	IFC_1210	IFC_1410
Form factor	6U VME64X	Double-width, mid-size (4HP) or full-size (6HP) MTCA.4
Height	233 mm	148 mm
Depth	160 mm	180 mm
Surface	373 cm^2	266 cm^2
Cooling	Air-cooled	Air-cooled
Live Insertion Capability	Yes	Yes (both AMC- and RTM-side)
Board Management	N/A	Yes (MMC)

Connectivity

Feature	IFC_1210	IFC_1410
VME	VME64x 2eSST	N/A
Ethernet	2x Gigabit Ethernet (CPU→FP)	2x Gigabit Ethernet (CPU→AMC) 2x Gigabit Ethernet (CPU→RTM) 2x 10Gig Ethernet (CPU→RTM)(*)
PCIe	VME P0 UHM: 1x 8-lane PCIe Gen2 or 2x 4-lane PCIe Gen2 or 4x 2-lane PCIe Gen2 or 8x 1-lane PCIe Gen2	2x 1-lane PCIe Gen2 (CPU→RTM)(*) 2x 4-lane PCIe Gen2 (FPGA→AMC)
User IO	112 IOs VME P2	4x point-to-point (FPGA→AMC) 4x shared bus MLVDS (FPGA→AMC) Up to 40 differential pairs (FPGA→RTM)

(*) 2x XFI and 2x PCIe are mutually exclusive. When using PCIe, the 4-lane PCIe link between the CPU and the Central FPGA is a Gen3. When using XFI, the link is a Gen2 due to T2081 limitations.

Extensibility

Feature	IFC_1210	IFC_1410
FMC slots	Dual VITA-57	Dual VITA-57 (with lower voltage VADJ)
XMC slots	Dual VITA-42.3	N/A (Single slot available on rear transition board RXI_1460)
PMC slots	Single IEEE P1386.1	N/A (Single slot available on rear transition board RXI_1460)
Rear IO	UHM P0 (7 Gbps)	4HP : dual ADF 30 differential pairs 6HP : dual ADF 40 differential pairs

CPU

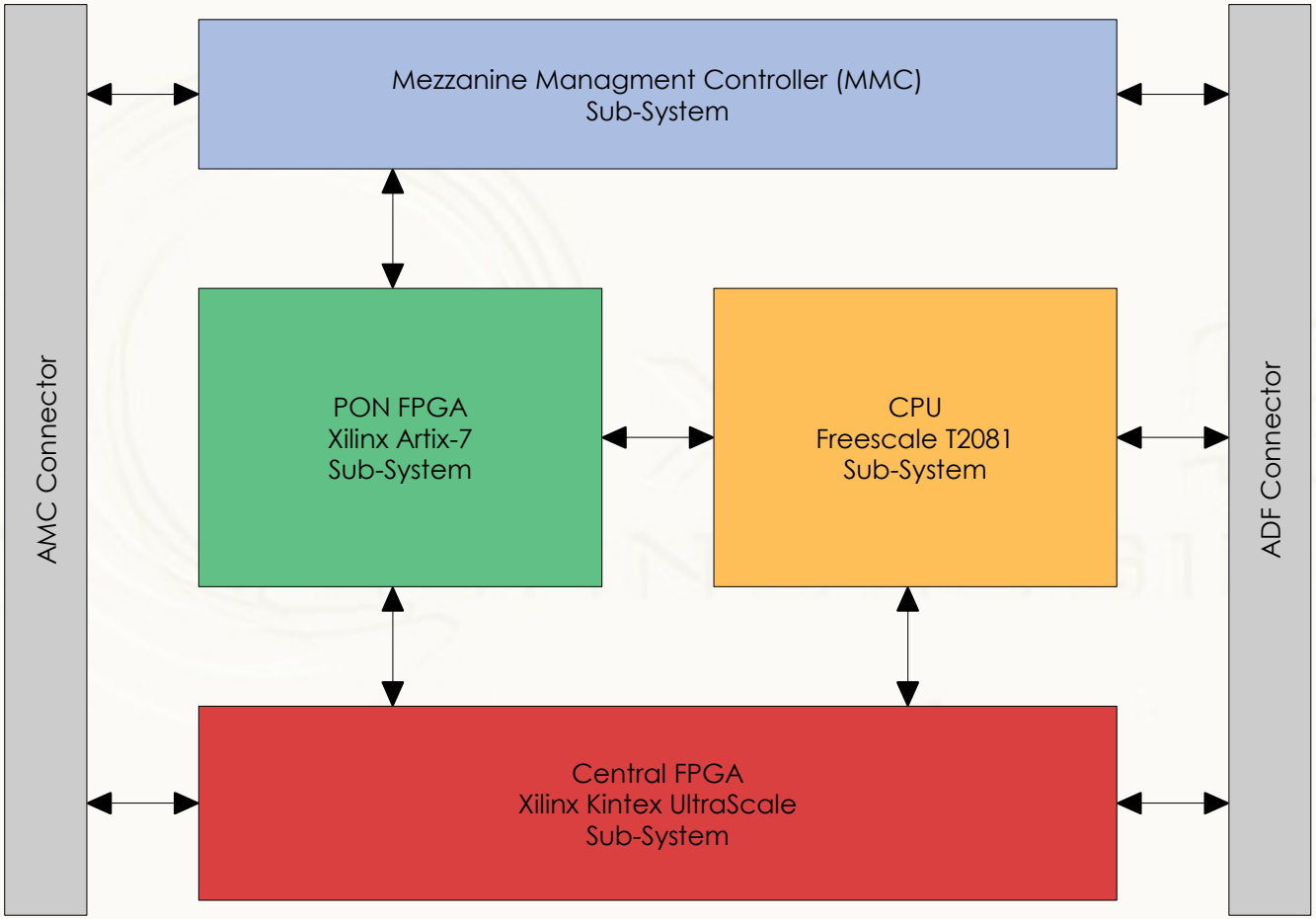
Feature	IFC_1210	IFC_1410
CPU	Freescale P2020 @ 1.2 GHz	Freescale T2081 @ up to 1.8 GHz
CPU SDRAM	Up to 2 GB on-board 64-bit DDR3-600 SDRAM with ECC	Up to theoretical 256 GB 64-bit DDR3-2133 SODIMM *without ECC*
Local storage	256 MB NAND flash	4 GB NAND flash (optional)
Non-volatile memories	16 MB NOR flash for CPU boot 16 MB NOR flash for FPGA config	64 MB NOR flash for CPU boot 128 MB SPI flash for FPGA config
Altivec	No	Yes
Floating Point	Software emulation	Hardware FPU

FPGA

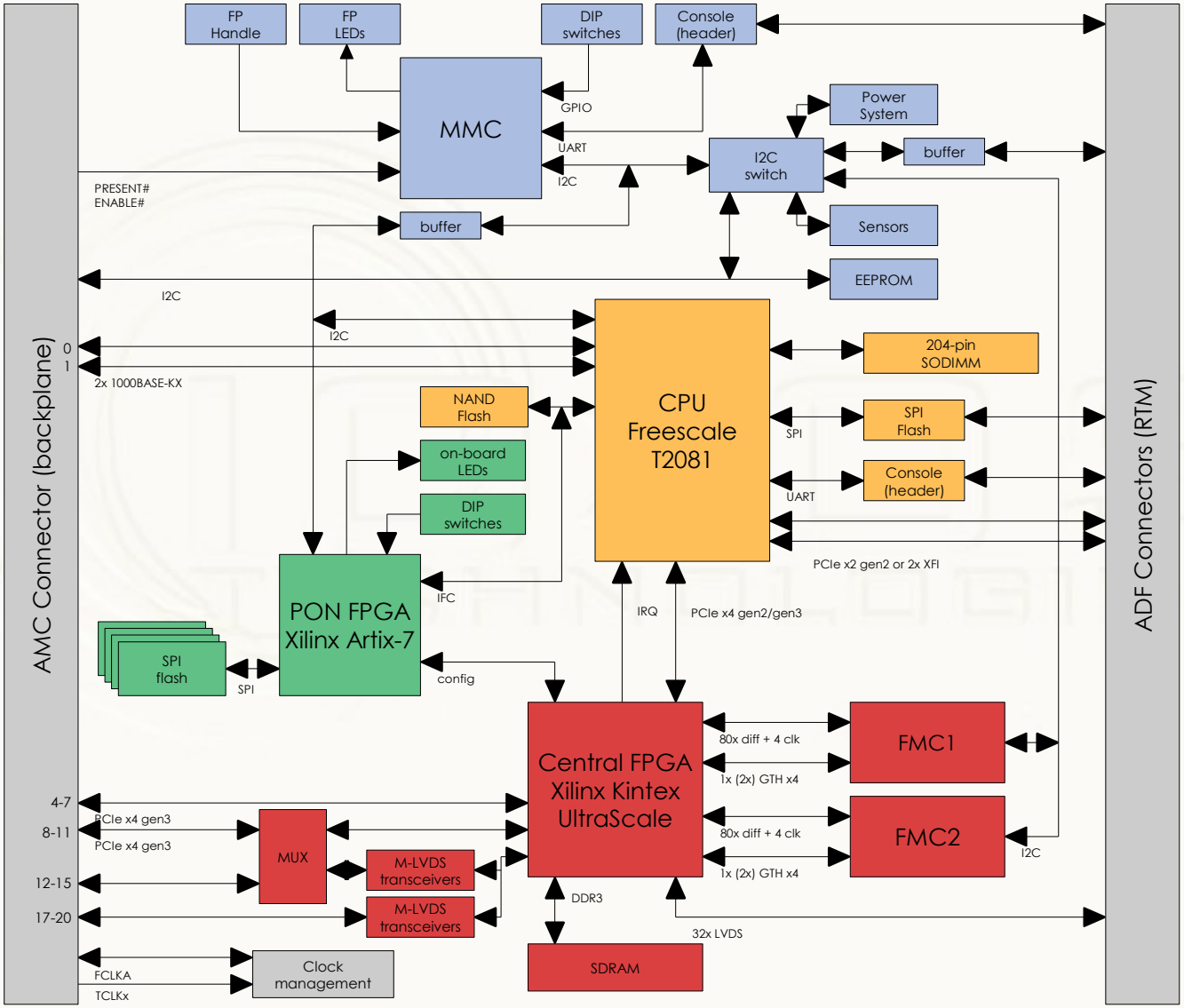
Feature	IFC_1210	IFC_1410
FPGA	Xilinx Virtex-6T LX130T (other devices available on demand)	Xilinx Kintex UltraScale KU040 (other devices available on demand)
LUTs	80'000	242'400
FFs	160'000	484'800
Distributed RAM	1.7 Mbits	7.0 Mbit
Block RAM	9.3 Mbits	21.1 Mbits
DSPs	480	1'920
MGTs	20 GTX @ 6.6 Gbps (-3, -2 speed grades) or 5 Gbps (-1)	20 GTH @ 16.3 Gbps (-3E, -2E, -2I speed grades) down to 10.3125 Gbps (-1LI speed grade)

IFC_1410 Architecture

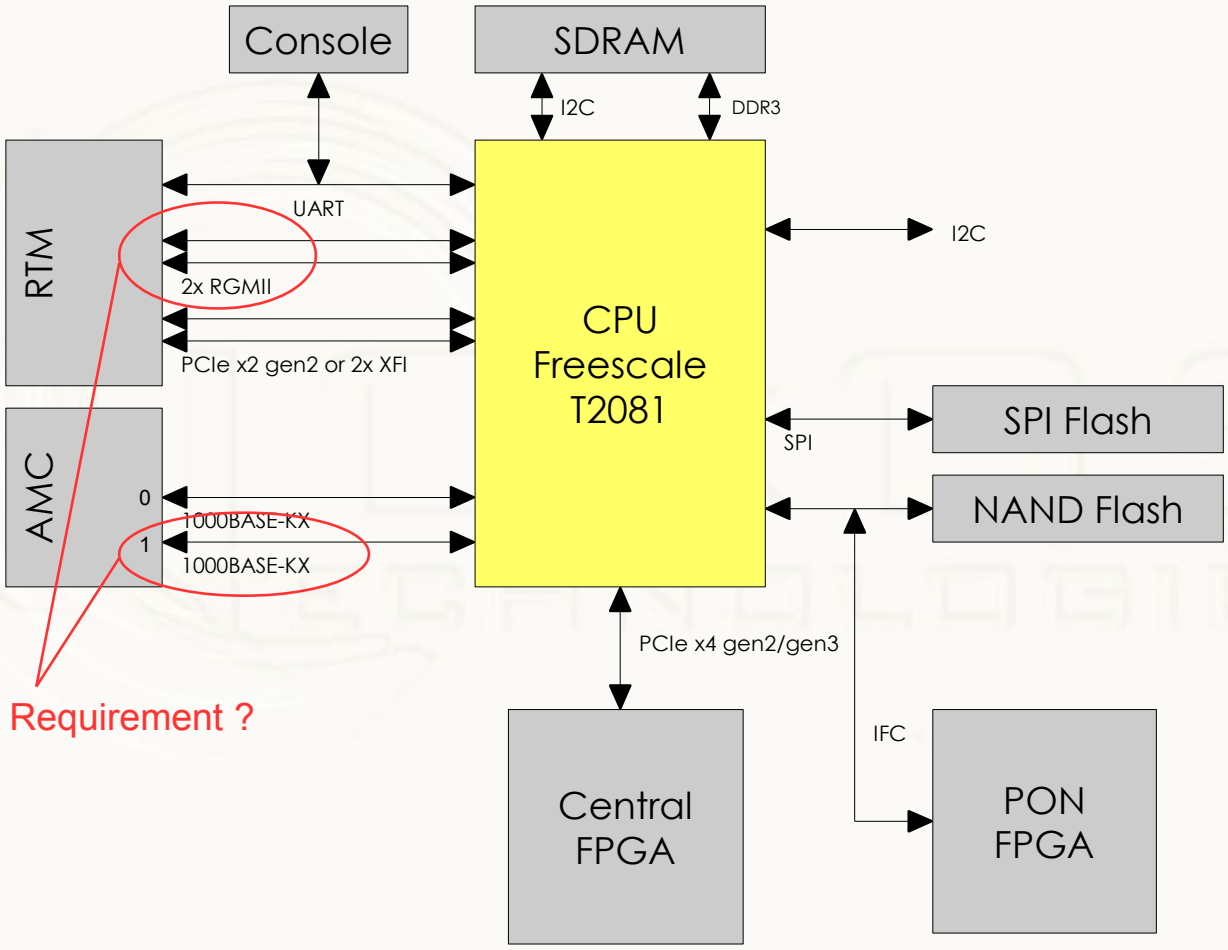
IFC_1410 : Block Diagram

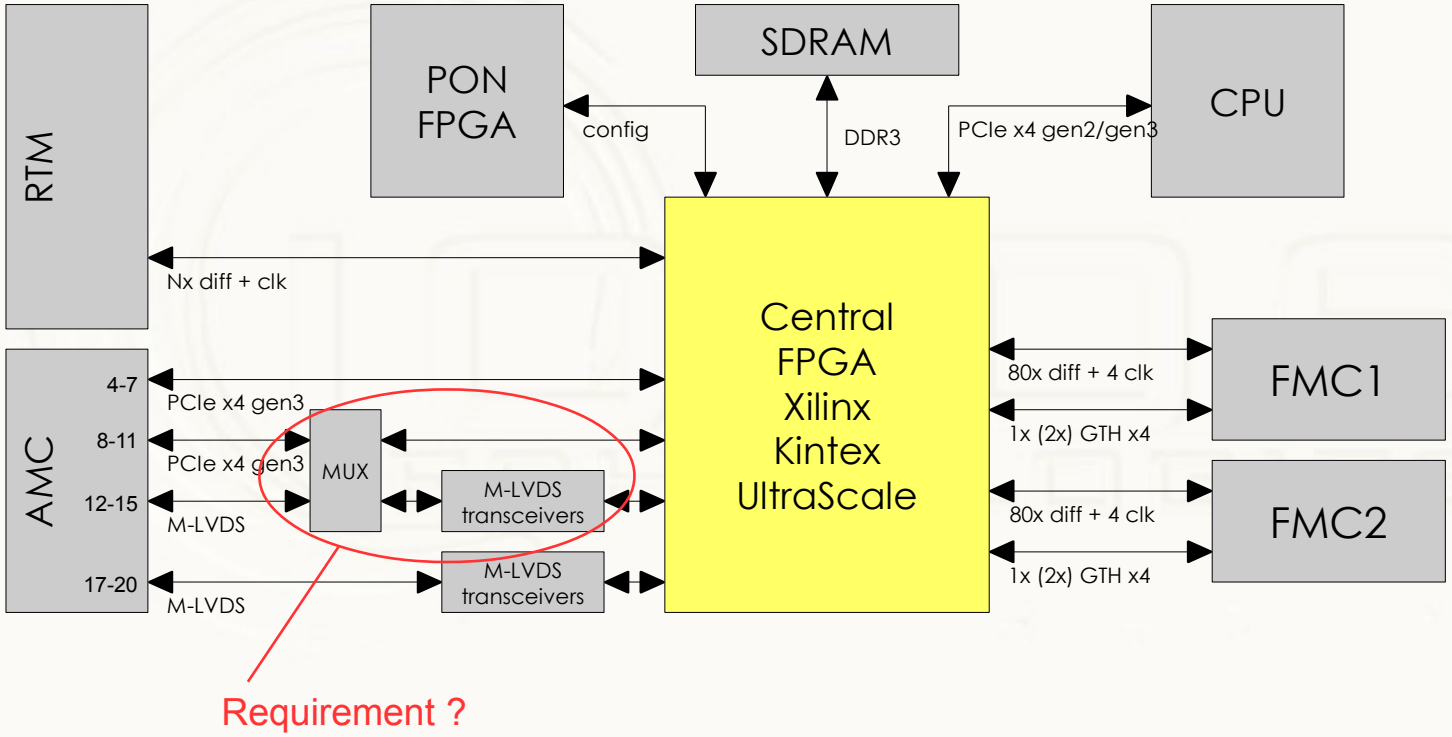


IFC_1410 : Block Diagram



IFC_1410 : CPU Sub-System

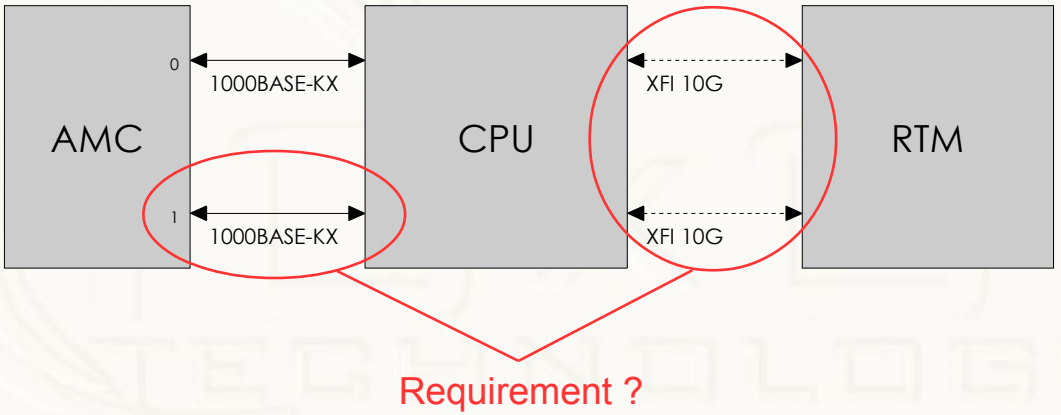



RTM
PON FPGA
SDRAM
CPU
config
DDR3
PCIe x4 gen2/gen3
Nx diff + clk
Central FPGA Xilinx Kintex UltraScale
AMC
4-7
8-11
12-15
17-20
PCIe x4 gen3
PCIe x4 gen3
M-LVDS
M-LVDS
MUX
M-LVDS transceivers
M-LVDS transceivers
80x diff + 4 clk
1x (2x) GTH x4
80x diff + 4 clk
1x (2x) GTH x4
FMC1
FMC2
Requirement ?

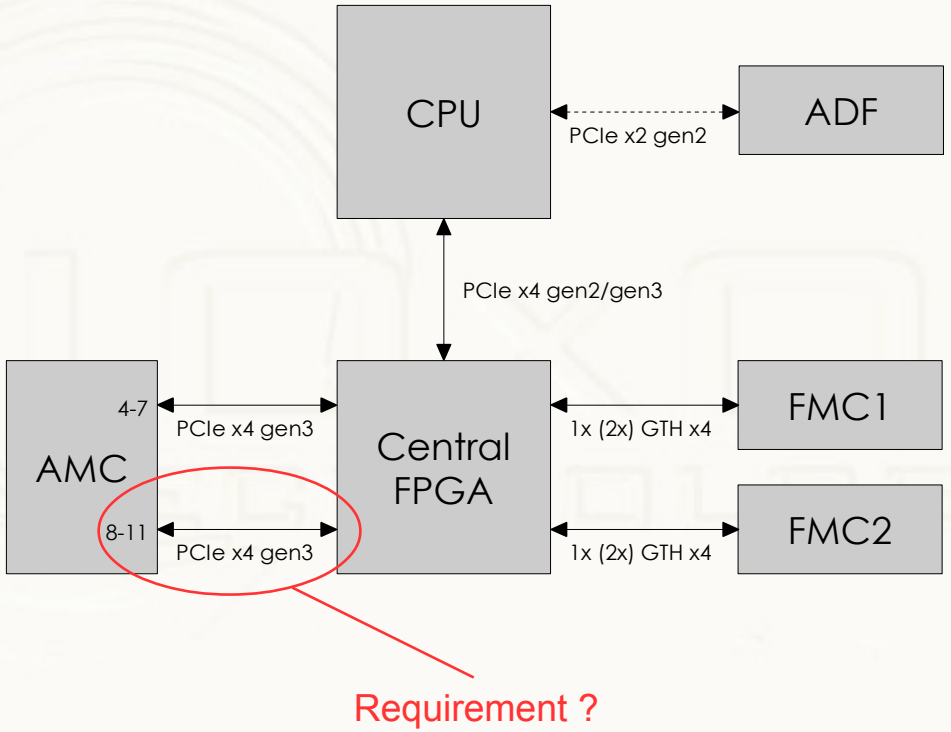
Why a Kintex UltraScale device ?

- 15-year end-of-life starting in 2015
- Multiple PCIe Gen3 endpoints
- 16 Gbps transceivers interesting for JEDS204B

IFC_1410 : Ethernet Connectivity



IFC_1410 : MGT Connectivity

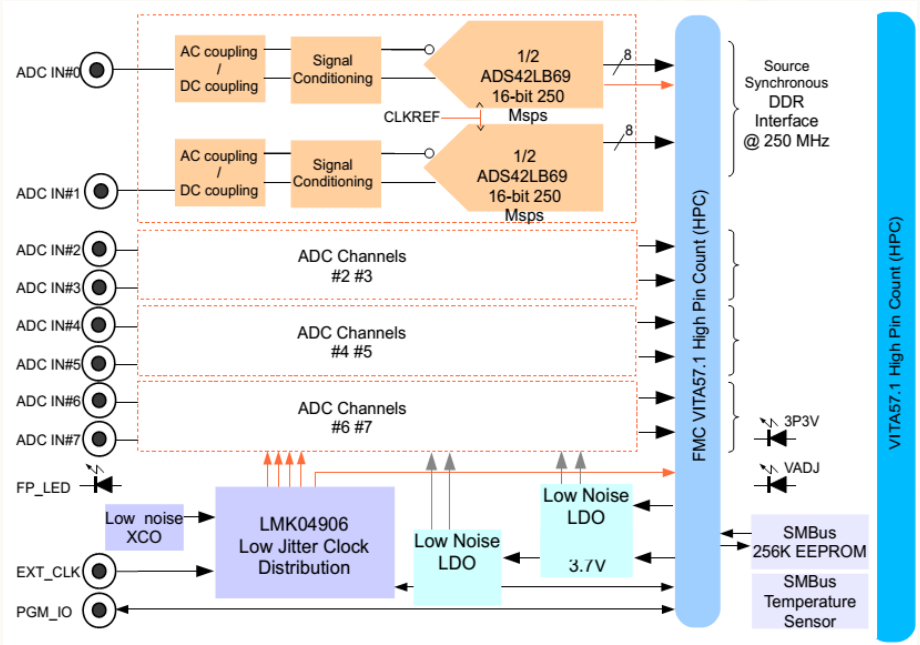


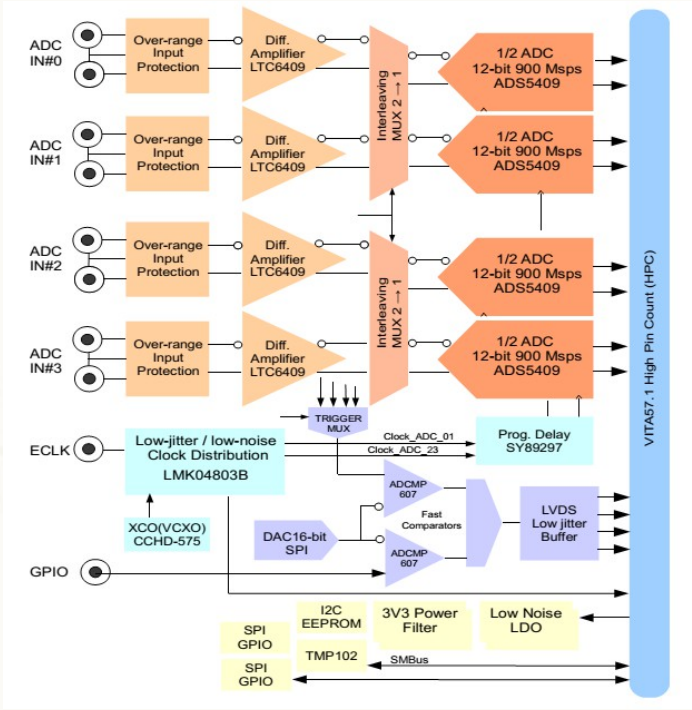
IFC_1410 Eco-System

Eco-System : Hardware

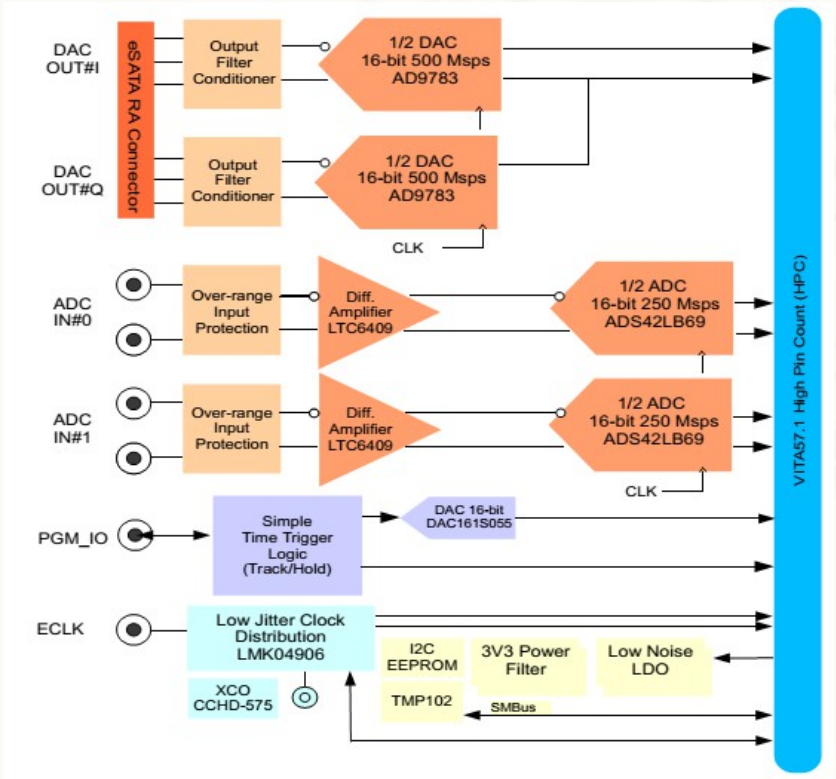
- The IFC_1410 is designed to be compatible with the IFC_1210
- Existing and future FMC products will be usable both on the IFC_1210 and IFC_1410

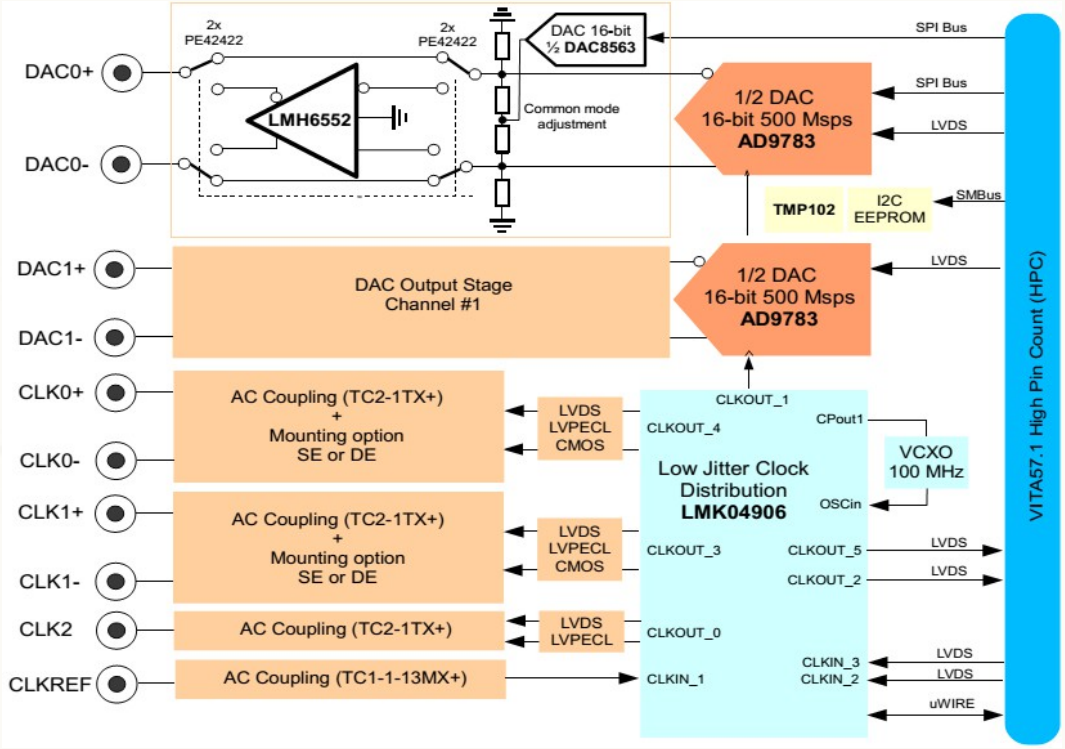
ADC_3110 / ADC_3112





DAC_3113 / DAC_3114





Eco-System : FPGA Design Kit

- The FPGA architecture is based on Tosca III Network on Chip environment, an evolution of Tosca II
- Applications developed for the IFC_1210 can be reused with minimal effort
- Existing applications will be available:
  - Waveform generator (DAC_3113)
  - Oscilloscope applications (ADC_3110/_3111)
  - LLRF / 16-bit ADC 250 Msps (ADC_3110)

Eco-System : Software

- The IFC_1410 will bootstrap from UBOOT, then run Linux
- IOxOS will provide all the necessary device drivers and tools to operate the IFC_1410
- Existing applications developed for the IFC_1210 will run on the IFC_1410

IFC_1420

- Same processing units as IFC_1410 (CPU & FPGAs)
- Single HPC VITA-57 FMC slot
- On-board ADC3110/ADC3111 function seen as a FMC
- DESY.A1-compliant ADF interface to supply the analog signals to the ADC function
- From the software and FPGA firmware standpoints, an IFC_1420 behaves like an IFC_1410 with an ADC3110/ADC3111 FMC

Rear Transition Module
RXI_1460
(previously known as RXI_1411)

Rear Transition Module

The exact functionality of the RXI_1460 rear-transition module is subject to discussion.

- Dual RJ45 Gigabit Ethernet ?
- Dual SFP+ 10Gig Ethernet ?
- PMC ?
- XMC ?
- SSMC for ultra-low jitter clock input ?

Conclusion