EUROPEAN SPALLATION SOURCE

FPGA design at ESS

Setting the future ESS Firmware design platform

State of the Art

The actual situation is:

- Each designer (in ESS or in the partner organization) uses is own tools, with different version and setting;
- The design folder structure is personally defined, like the type of required documentation;
- There is no quality control on the actual designed FPGA: i.e. golden model of many system is not yet available to provide information for acceptance of the code, or to automatize the simulation, or the testing;
- There is not defined contract clause for the firmware design, that fix boundaries for the designer of in-kind partners;
- there is no catalogue of already designed block with proper documentation, that allows a reuse of code;
- There is no floorplanning approach to the design of the actual project.

Central server for firmware design

- ESS is part of EUROPRACTICE license (R22140 for Accelerator, R21990 for Neutron), ICS is the real proprietary of the Firmware design;
- all the FPGA design are in a selected repository (BITBUCKET);
- we need to set up a central server, available to all the FPGA designer (in ESS and in-kind), to unify the bitstream generation.

Unique toolchain

Different Virtual Boxes, or Virtual Machines, should be created for specific AMC boards (STRUCK, IOxOS, Vadatech, etc…), with

- ✓ a specific implementation settings;
- ✓ a specific version of the tool (ISE for the Virtex6, VIVADO for the Kintex UltraScale);
- ✓ A set of script (like HDLMake from CERN) should be created, to allow automatic implementation when a new code is push in the repository, and provide the results via mail to the designer;
- ✓ The specific version of the used tools itself had to be in the repository, to allow repeatability of code generation.

Folder structure

It is important, for future support, that a specific folder structure is defined for the firmware code, modeling, benchmarking, documentation and scripts, so in any moment and different people should be able to perform support for any project;

NOTE: code should be properly commented and written to allow other designer to understand the functionality implemented

Quality control

Especially for in-kind is necessary to define strict guidelines on how the code had to be designed, and what are the acceptance condition:

- When is applicable (especially in BI) is necessary to provide a model (normally called GOLDEN Model), that provide
  - ✓ expected and tested functionality in a different language (like C, MATLAB, PERL. Etc..);
  - ✓ a specific set of scenarios of input data (that represent a well known set of problems or necessary to evaluate the function performance);

This approach allow to test the design, verify the performance and improve the maintainability in the future.

Firmware catalogue

All the design on a specific AMC share at least the general framework(e.g. TOSCA for IOxOS) and could be some specific function or DSP;

- Should be created a catalogue of all these part (IPs), and discussed the portability between the different platform;
- To improve the design time and the quality of the bitstream, it should be applied a floorplanning approach to this IP.

Conclusion

It is necessary to define:

- How to proceed on this proposal;
- Who is in charge for the various point proposed;
- When the various part become available, and how to maintain it;