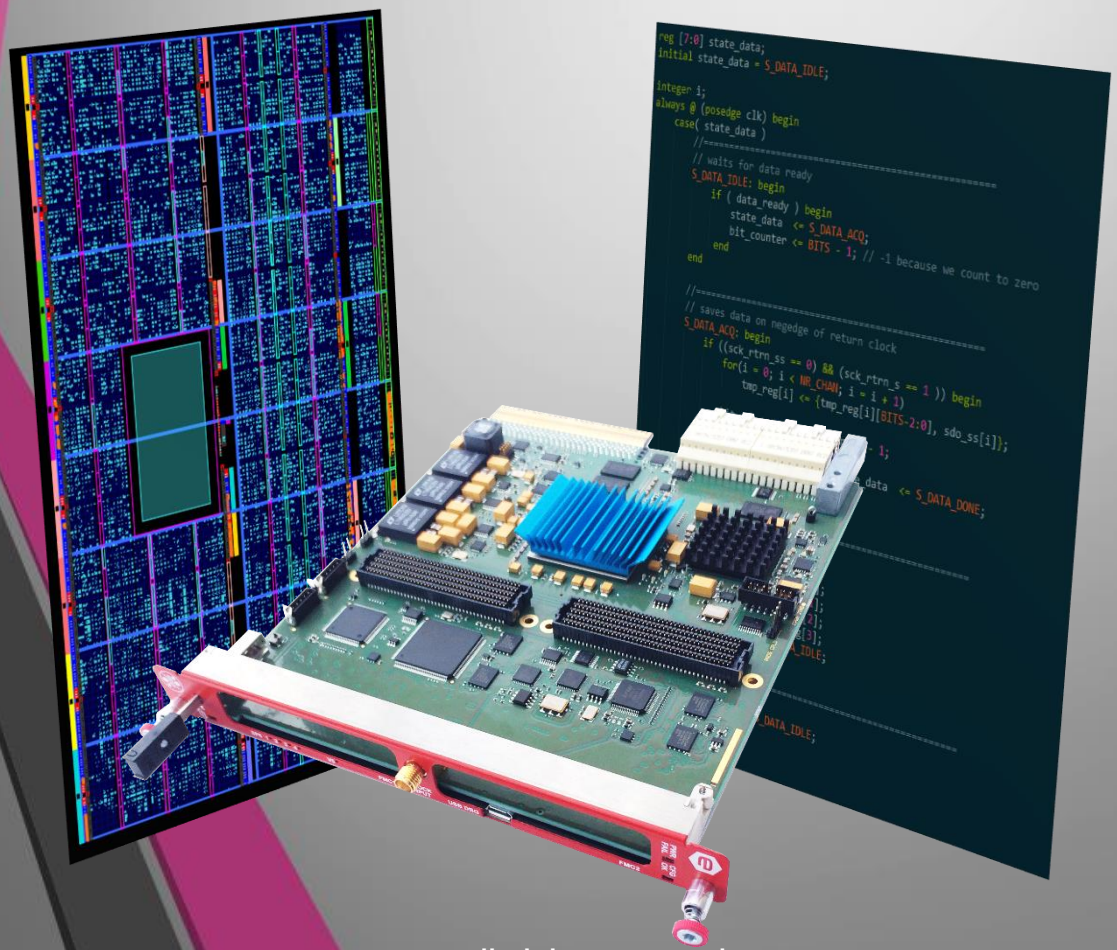
DAMC-FMC25

AMC Dual High Pin Count FMC Carrier Board

CAENels
Gear for Science

Board Support Package Overview



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MTCA.4 – MicroTCA for Physics

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Document Revisions

Document Revision	Date	Comment
1.0	September 9th 2015	First Release

1. Introduction

This document describes the DAMC-FMC25 Board Support Package. The core of the system is the Virtex-5 FPGA, which provides backplane connectivity (PCI express on ports 4-7, low latency links on ports 12-15), connections to both FMC boards, connection with the on-board DDR2 memory (to store the data) and the PowerPC 440 processor which can be used as a board supervisor.

The board support package heavily relies on AXI protocol. The AXI4-Lite and AXI4-Stream are widely used protocols in FPGAs and offer flexible and easy-to-implement interface between modules. AXI4-Lite is used for reading and writing to control and status registers in the FPGA modules, while AXI4-Stream is used for data streams (such as fast measurement data flow). The board support package contains 3 Bus Functional Models (AXI4-Lite slave, AXI4-Lite master and AXI4-Stream master), which are used to exercise the AXI components in simulation.

The following block diagram shows basic components of the Virtex-5 BSP.

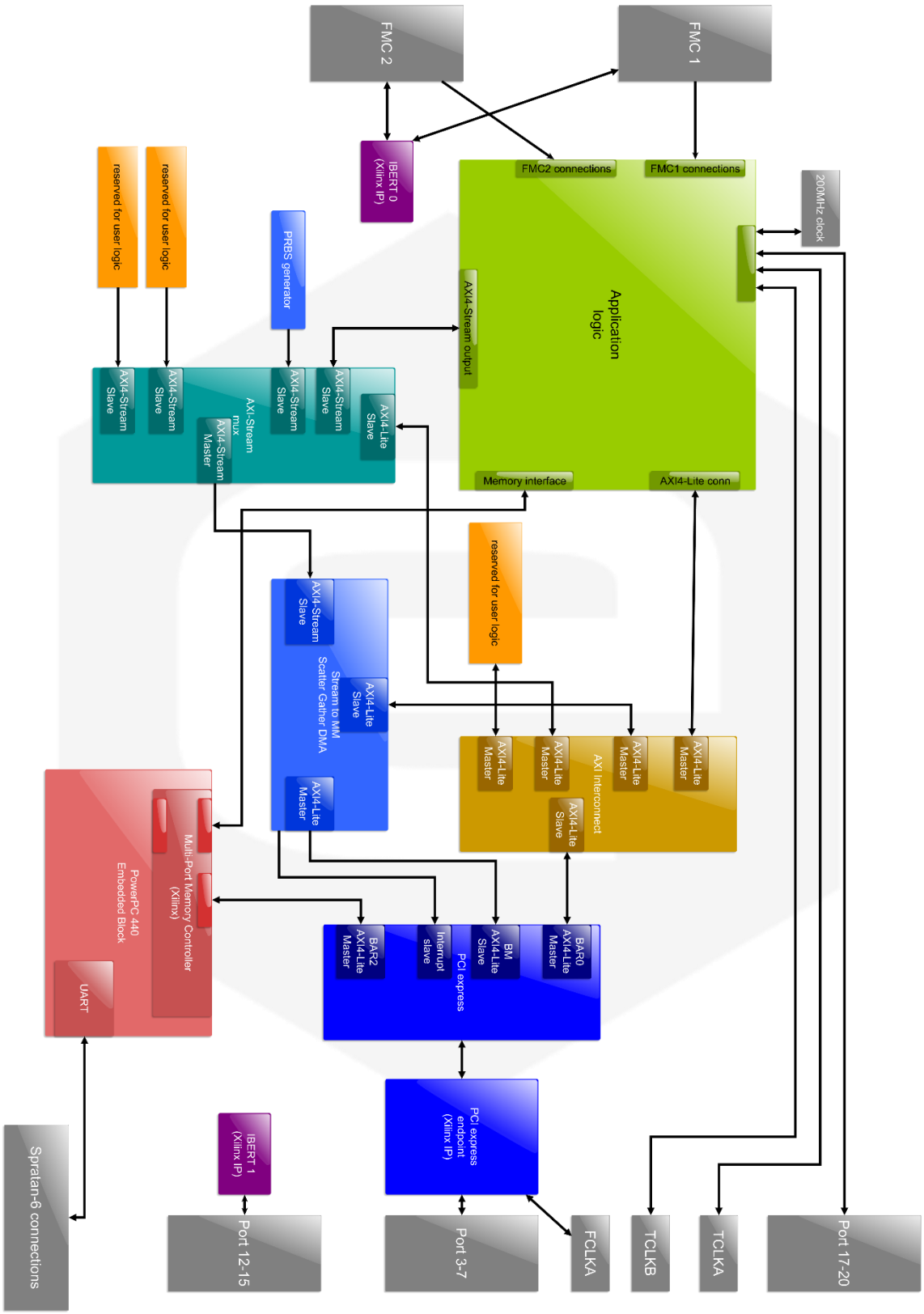

Figure 1: BSP Overview

1.1 PCI express

This module translates PCI express Transaction Layer Protocol memory read (MRd) and memory write (MWr) request to requests on AXI bus. The BAR0 and BAR2 are the AXI-4 Lite Masters with 32-bit data and address bus. The BAR0 is used to read and write to control and status registers in other FPGA modules. The BAR2 is connected to Multi-Port Memory Controller, which offers access to DDR2 memory and handles the arbitration between various ports.

The Bus Master interface can be used together with the DMA to transmit large quantities of data to PCIe Root Complex (e.g. CPU or another PCIe board). This feature is extremely useful to quickly transmit the measurement data out.

1.2 AXI Interconnect

The AXI Interconnect module provides a memory mapping between the 4 slave modules (connected to the AXI4-Lite Master ports) and one master interface (connected through the AXI4-Lite Slave port to the BAR0). The addresses are provided as module parameters and can be set before the synthesis. If the address decoder is unable to decode the read requests, the magic number 0xBADADD75 (“Bad Address”) is returned on data channel.

1.3 Scatter-Gather DMA

The DMA (Direct Memory Access) module transfers the data stream from reduced AXI4-Stream slave port (with data, strobe, ready and valid signal) to memory mapped accesses to PCI express module. This advanced implementation of DMA allows queuing of commands, which can be used to write a continuous stream of data to several non-continuous memory location (a common situation with x86 processor with Memory Management Unit). See AMC-Pico-8 User's Manual for detailed description.

1.4 AXI-Stream Mux

The AXI-Stream Mux is a module which connects one of the stream input channel to the stream output channel. The connection is set in the configuration register, accessible from AXI4-Lite slave. The data, strobe and valid signals are connected from input to output, while the ready signal is connected from output to input.

1.5 IBERT cores

The Xilinx IBERT (Integrated Bit Error Ratio Test) cores allow to evaluate and test the high speed links such as low-latency point-to-point links on backplane (ports 12-15) and the dedicated transceiver connection on FMC board.

The following figure displays the use of IBERT module together with FMC-2SFP+ board, optical SFP and 10 m of optical fibre cable.

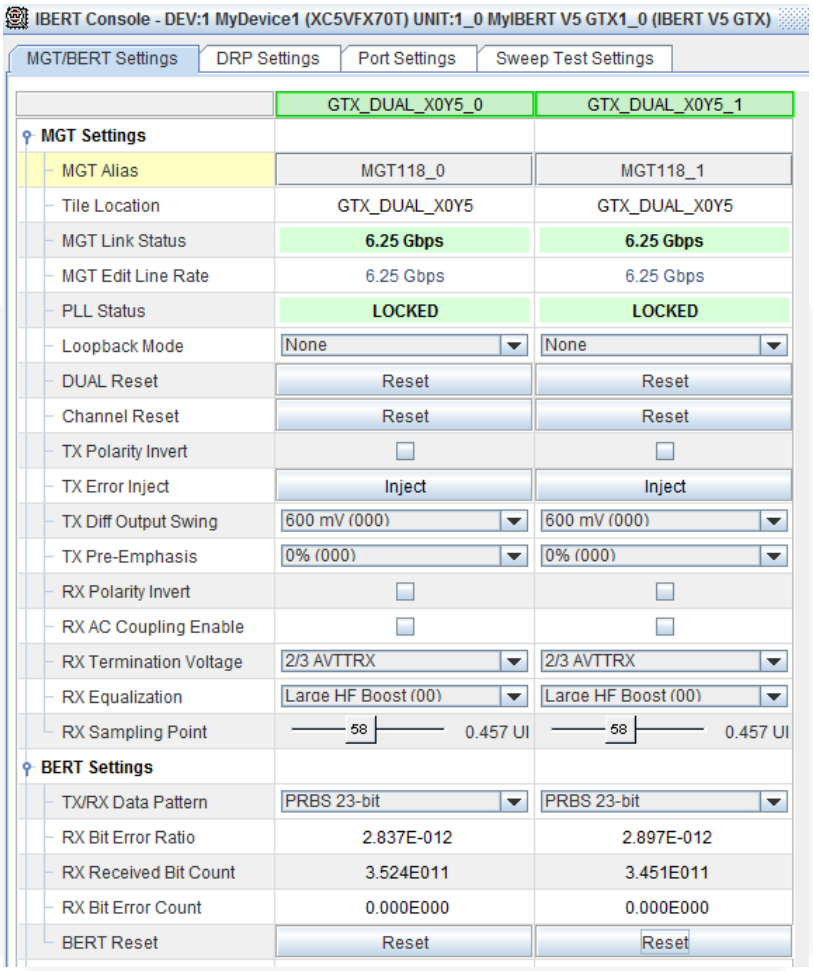

Figure 2: IBERT link test

1.6 PowerPC 440 block

The Virtex-5 embeds a powerful PowerPC440 processor. It can be used to implement the various software tasks, e.g. system supervisor, TCP server, Web server or control system server. The Yocto Project also provides a port of Linux, see http://git.yoctoproject.org/cgit/cgit.cgi/meta-xilinx-community.

The following image shows the basic XPS (Xilinx Platform Studio) system with PowerPC core, DDR2 memory, UART interface, local memory, and timer. It can be further extended with IP cores provided by Xilinx (e.g. Ethernet interface) and custom cores for user specific application.

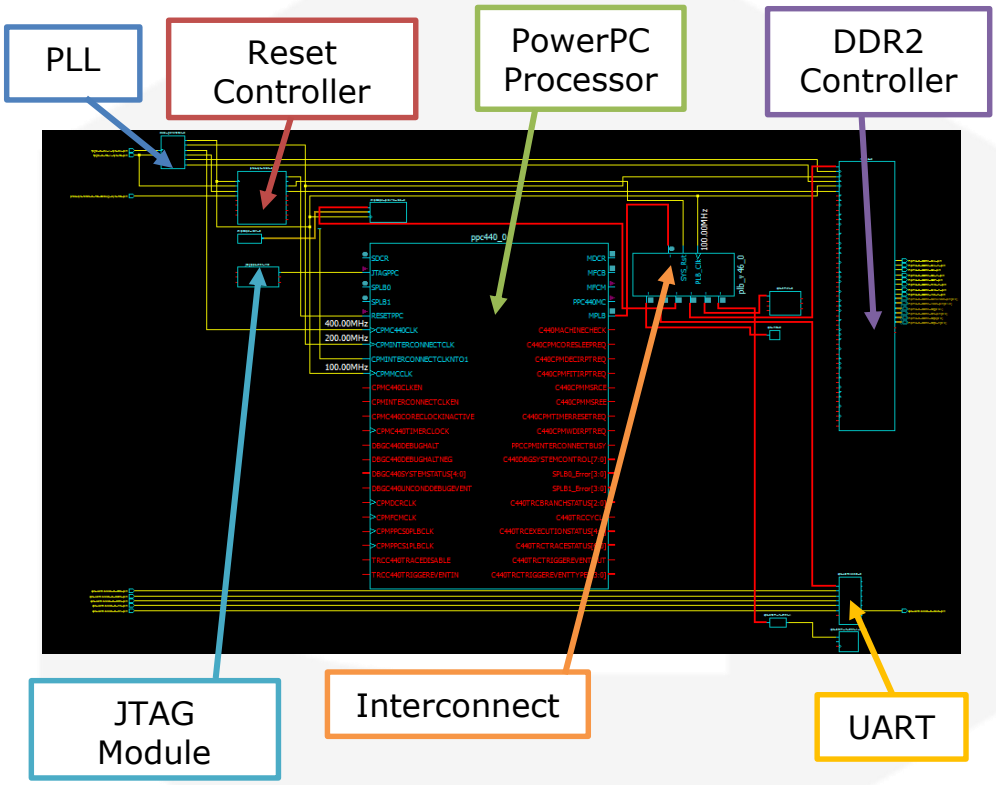

Figure 3: PowerPC system

1.6.1 Software

Included in BSP is a test program which verifies the DDR2 memory. The following image shows the results of the test.

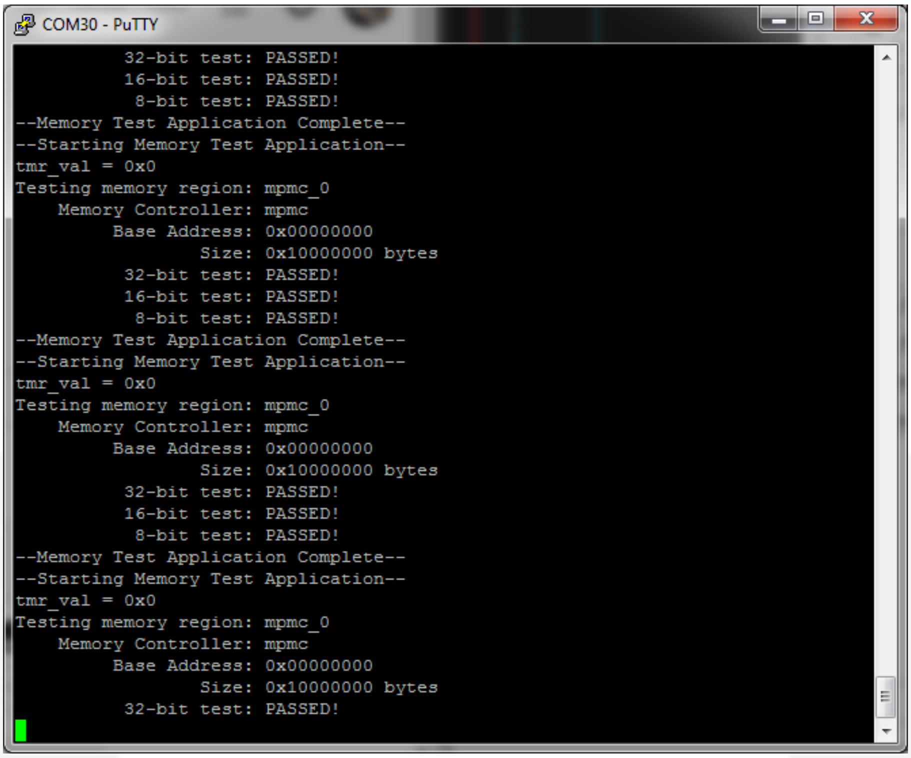

Figure 4: DDR2 memory test

2. Address map

2.1 AXI DMA (address 0x0001 0000)

2.1.1 Status (0x00)

Bit	Name	Access	Description
26:16	RESP_COUNT	R	Number of responses in response FIFO
14:4	CMD_COUNT	R	Number of commands in command FIFO
0	TRANS_IN_FLY	R	DMA engine is performing transfer

2.1.2 Control (0x04)

Bit	Name	Access	Description
8	ENGINE_ENABLE	R/W	Enables or disables DMA engine
0	RESET_ENGINE	W	Resets the current DMA transfer

2.1.3 Command (0x08)

Bit	Name	Access	Description
31	GO	W	Puts command in command FIFO
27	IRQ_ENABLE	W	Generates interrupt when DMA transfer finished. It should be set in the same cycle as GO bit.

2.1.4 Command address (0x0C)

Bit	Name	Access	Description
31:0	CMD_ADDR	R/W	DMA command address

2.1.5 Command length (0x10)

Bit	Name	Access	Description
31:0	CMD_LENGTH	R/W	DMA command length (bytes)

2.1.6 Response length (0x14)

Bit	Name	Access	Description
31:0	RESP_LENGTH	R/WtoP	Number of byte transferred. Write to pop from response FIFO.

2.1.7 Response address (0x18)

Bit	Name	Access	Description
31:0	RESP_ADDR	R	Starting address of DMA transfer.

2.2 AXI Stream Mux (address 0x0002 0000)

2.2.1 Output selector (0x0)

Bit	Name	Access	Description
1:0	OUT_SEL	R/W	Selects the input to be connected to the output port.

3. File list

3.1 Virtex-5

```
damc25-virtex
├── constraints
│   ├── pin_assigments.ucf
│   └── timing_costraints.ucf
├── edk
│   ├── SDK
│   │   └── SDK_Export
│   │       ├── edk_hw_platform
│   │       │   └── system.xml
│   │       ├── mem_test
│   │       │   └── src
│   │       │       ├── lscript.ld
│   │       │       ├── memory_config.h
│   │       │       ├── memory_config_g.c
│   │       │       ├── memorytest.c
│   │       │       ├── platform.c
│   │       │       ├── platform.h
│   │       │       └── platform_config.h
│   │       └── standalone_bsp_0
│   │           ├── libgen.log
│   │           ├── libgen.options
│   │           ├── Makefile
│   │           └── system.mss
│   ├── ppc_system.mhs
│   └── ppc_system.xmp
├── hdl
│   ├── application_logic
│   │   └── pll_300.v
│   ├── axi_dma
│   │   ├── test
│   │   │   ├── axi_dma_tb.sv
│   │   │   └── sim.do
│   │   ├── axi_dma.v
│   │   ├── axi_dma_control_slave.v
│   │   └── axi_dma_engine.v
│   ├── axi_interconect
│   │   ├── test
│   │   │   ├── axi_interconnect_tb.sv
│   │   │   └── sim.do
│   │   ├── axi_interconnect.v
│   │   ├── axi_interconnect_addr_dec_read.v
│   │   ├── axi_interconnect_addr_dec_write.v
│   │   ├── axi_interconnect_master.v
│   │   ├── axi_interconnect_master_read.v
│   │   ├── axi_interconnect_master_write.v
│   │   ├── axi_interconnect_slave.v
│   │   ├── axi_interconnect_slave_read.v
│   │   └── axi_interconnect_slave_write.v
│   ├── axis_dummy
│   │   └── axis_dummy.v
│   ├── axis_mux
│   │   ├── axis_mux.v
│   │   ├── axis_mux_control.v
│   │   └── axis_mux_logic.v
│   ├── axis_prbs
```

```
│   │   ├── test
│   │   │   ├── prbs32.c
│   │   │   └── sim.do
│   │   ├── axis_prbs.v
│   │   └── PRBS32.v
│   ├── pcie_axi_sys
│   │   ├── test
│   │   │   └── pcie_axi
│   │   │       ├── pcie_axi_tb.sv
│   │   │       └── sim.do
│   │   ├── pcie_axi.v
│   │   ├── pcie_axi_functions.v
│   │   ├── pcie_axi_master.v
│   │   ├── pcie_axi_slave.v
│   │   ├── pcie_axi_sys.v
│   │   ├── pcie_int_ctrl.v
│   │   └── README.md
│   ├── application_pico.v
│   ├── DAMC25_virtex_top.v
│   └── user_logic.v
├── ipcore_dir
│   ├── coregen.cgp
│   ├── endpoint_blk_plus_v1_15.xco
│   ├── fifo_dma_queue.v
│   ├── fifo_dma_queue.xco
├── project
│   └── placeholder_for_project_dir.txt
├── scripts
│   └── recreate_project.tcl
├── test
│   ├── bfms
│   │   ├── axi_master_bfm.sv
│   │   ├── axi_slave_bfm.sv
│   │   ├── axis_master_bfm.sv
│   │   └── README.md
│   ├── mytimeout.sh
│   └── run_all_test.sh
├── README.md
├── test_build_master_branch.sh
└── ver_ts_const.h
```

3.2 Spratan-6

```
damc25-spartan
├── constraints
│   ├── pin_assigments.ucf
│   └── timing.ucf
├── hdl
│   ├── crosspoint_switch
│   │   ├── crossbar_switch.v
│   │   ├── crossbar_switch_tb.sv
│   │   └── sim.do
│   └── damc25_spartan.v
├── project
│   └── placeholder_for_ISE.txt
├── scripts
│   └── damc25-spartan.tcl
└── README.txt
```