EUROPEAN SPALLATION SOURCE

ESS FPGA development framework

with application to BI instrumentation

ESS FPGA development framework

- FPGA introduction for dummies
- ESS platform
- ESS DEVENV for IKCs
- nBLM

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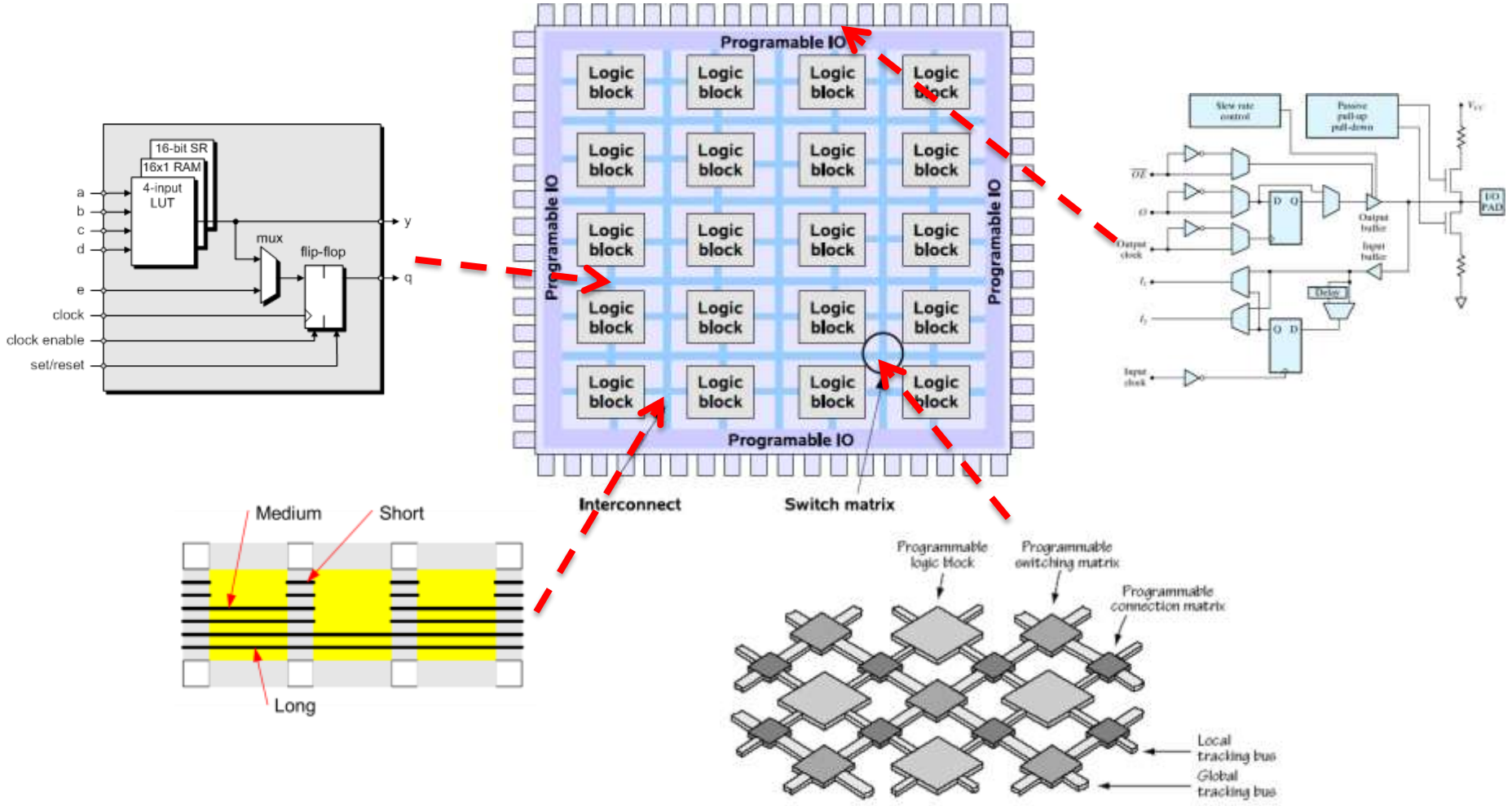
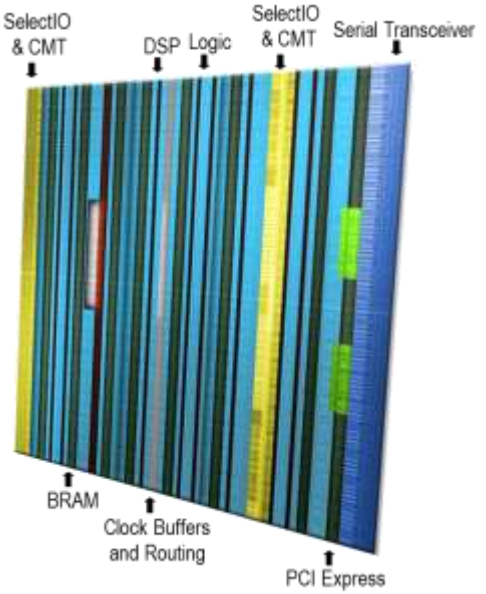
FPGA Architecture



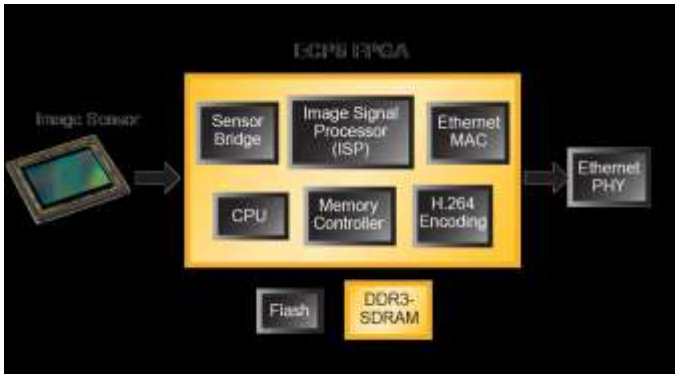
FPGA Architecture

Contemporary FPGA architectures incorporate the basic elements along with additional computational and data storage blocks that increase the computational density and efficiency of the device.

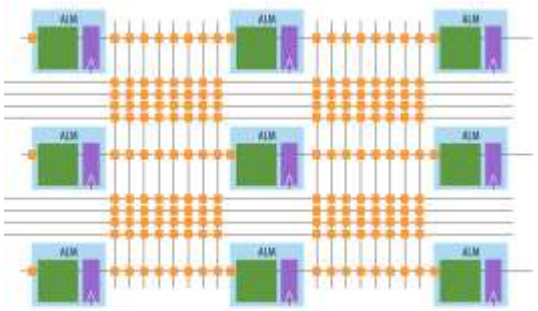
The combination of these elements provides the FPGA with the flexibility to implement any software algorithm running on a processor.



XILINX



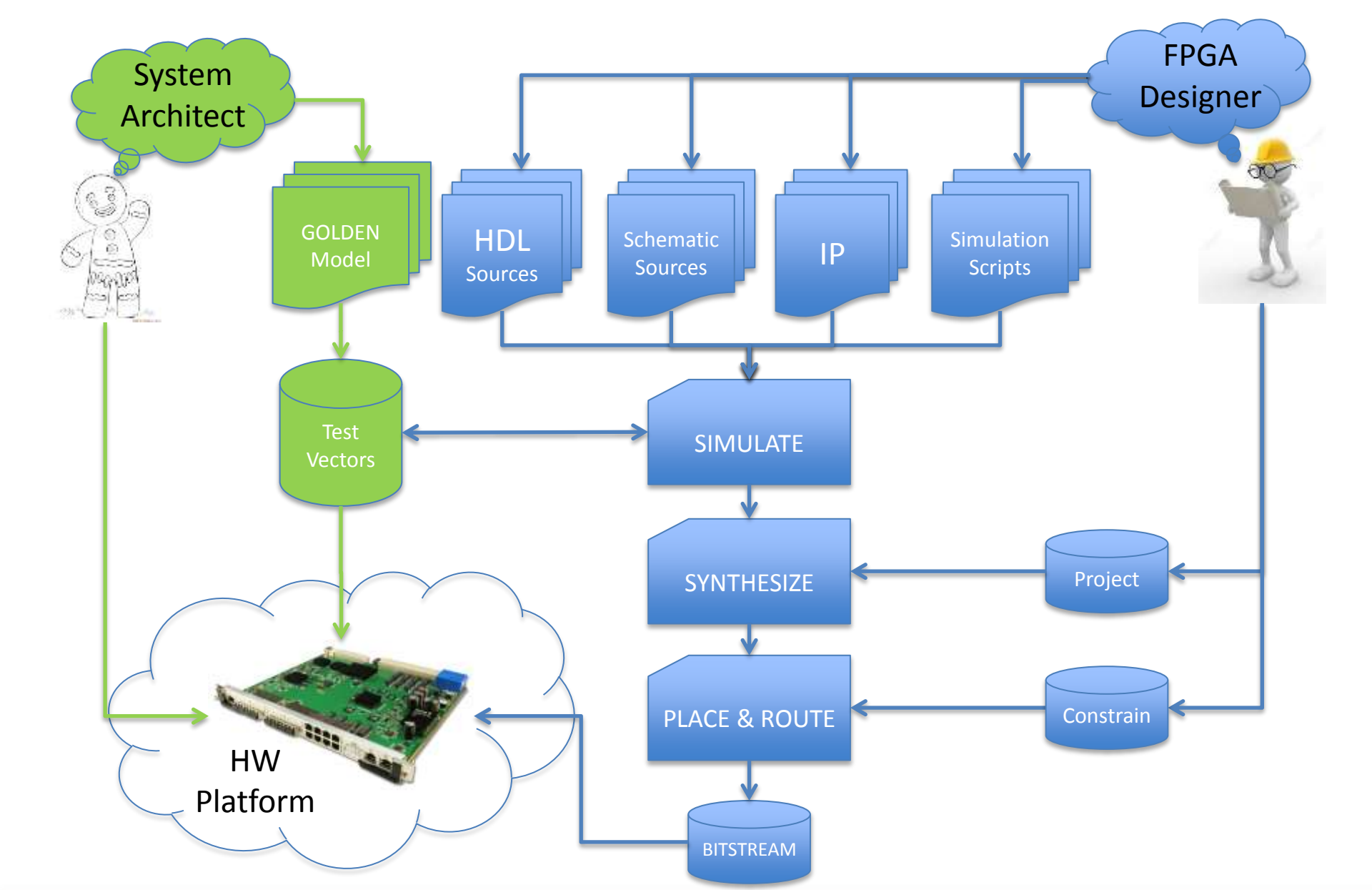
LATTICE SEMICONDUCTOR



ALTERA

Hardware Description Language - Introduction

- HDL is a language that describes the hardware of digital systems in a textual form.
- It resembles a programming language, but is specifically oriented to describing **HARDWARE STRUCTURES** and **BEHAVIORS**.
- The main difference with the traditional programming languages is HDL's representation of **extensive parallel operations** whereas traditional ones represents mostly serial operations.
- The most common use of a HDL is to provide an alternative to schematics.


System Architect
FPGA Designer
GOLDEN Model
HDL Sources
Schematic Sources
IP
Simulation Scripts
Test Vectors
SIMULATE
SYNTHESIZE
Project
PLACE & ROUTE
Constrain
BITSTREAM
HW Platform

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Beam Diagnostics

The Beam Diagnostics work package includes the development of all beam instrumentation for the ESS linac:

- BLM (Beam Loss Monitor)
- BCM (Beam Current Monitor)
- BPM (Beam Position Monitor)
- FC (Faraday Cup)
- WS (Wire Scanner)
- NPM (Non-Invasive Profile Monitor)
- EMU (Emittance Measurement Unit)
- LBM (Longitudinal Bunch Profile Monitor)

etc…..

Integrated Control System (ICS)

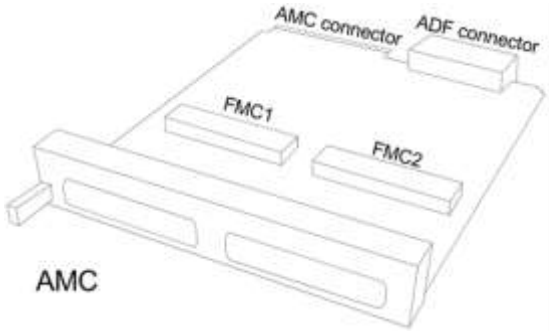
The ESS Control System is a complex network of hardware, software and configuration databases that integrates the operations of all the various parts of the Accelerator, Target, Instrument and Conventional Facility infrastructures.

ESS has a large network of laboratories to exchange knowledge, personnel and experience with, and that in many cases will contribute directly to the project through **In-Kind Contributions (IKCs)**

MTCA.4 AMC

BEAM DIAGNOSTIC
PROTOTYPE
PLATFORM

MIGRATION



PAUL SCHERRER INSTITUT
PSI
IOxOS TECHNOLOGIES

KINTEX UltraSCALE

ICS
FINAL
PLATFORM

FPGA comparison

DAMC-FMC25 (VIRTEX-5)																
Device	Configurable Logic Blocks (CLBs)			DSP48E Slices	Block RAM			Blocks CMTs	PowerPC Processor	Blocks Endpoint Blocks for PCI Express	Ethernet MACs	Max RocketIO Transceivers		Total I/O Banks	Max User I/O	
	Array (Row x Col)	Virtex-5 Slices / LUTs FFs	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)					GTP	GTX			
XC5VFX70T	160 x 38	11,200 / 44,800	820	128	296	148	5,328	6	1	3	4	N/A	16	19	640	~1/2

SIS8300-L (VIRTEX-6)																
Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices	Block RAM Blocks			MMCMs	/	Interface Blocks for PCI Express	Ethernet MACs	Maximum Transceivers		Total I/O Banks	Max User I/O	
		Slices	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)					GTP	GTX			
XC6VLX130T	128,000	20,000	1,740	480	528	264	9,504	10	/	2	4	20	0	15	600	1

Kintex UltraScale FPGA																
	System Logic Cells	CLB FFs / CLB LUTs	Maximum Distributed RAM (Mb)	DSP Slices		Block RAM/FIFO w/ECC (36Kb)	Total Block RAM (Mb)	CMTs (1 MMCM, 2 PLLs)		PCIe Gen3 x8		GTH 16.3Gb/s Transceivers				
KU040	530,250	484,800 / 242,400	5.9	1,920		600	19.0	10		3		20				~5

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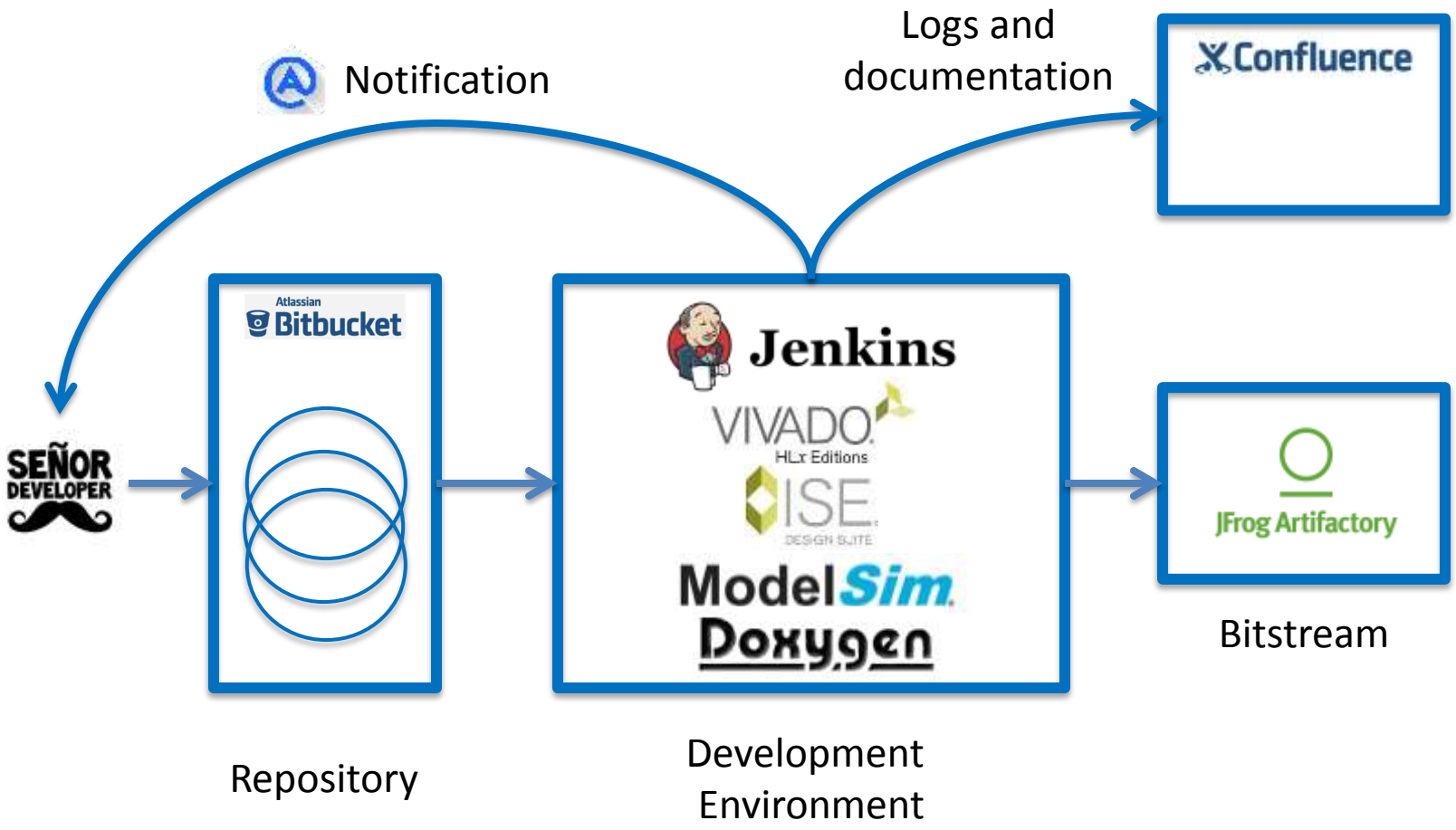
ICS Continuous Integration/Delivery

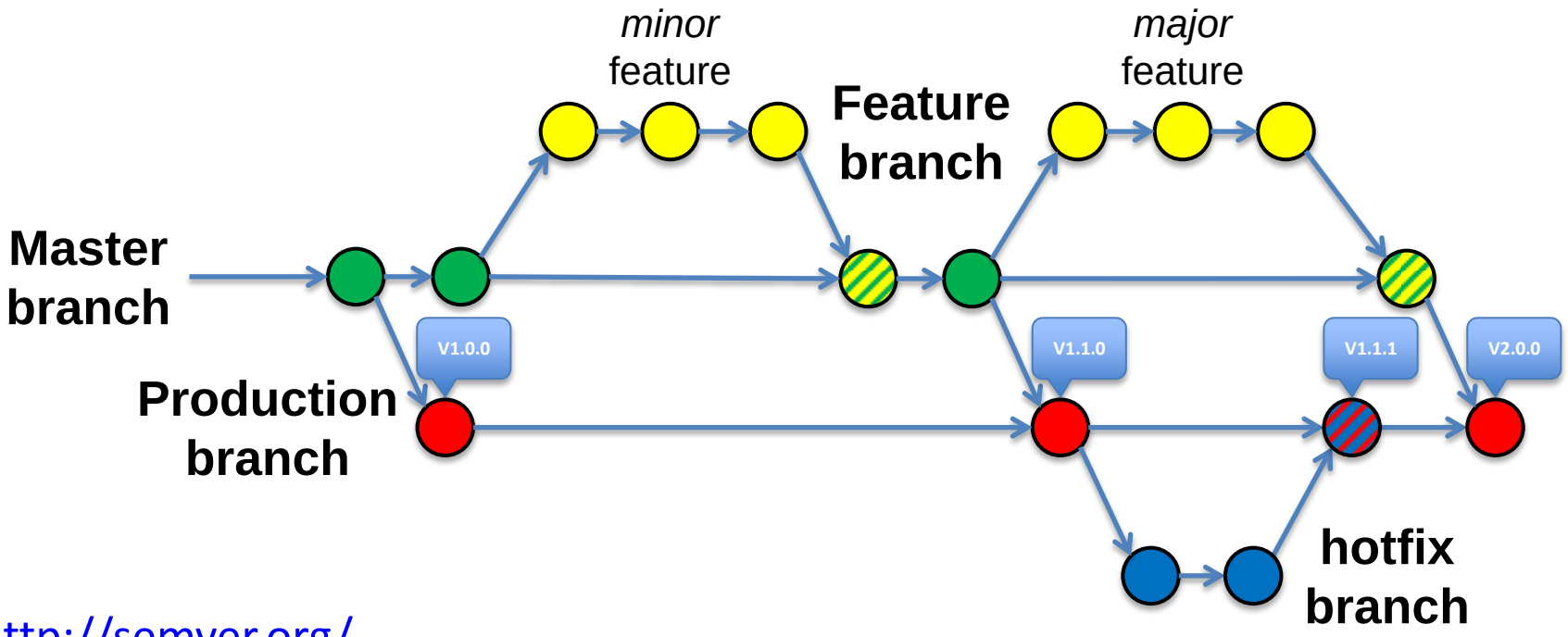
Courtesy of Leandro Fernandez

JAVA flow

FPGA design/delivery



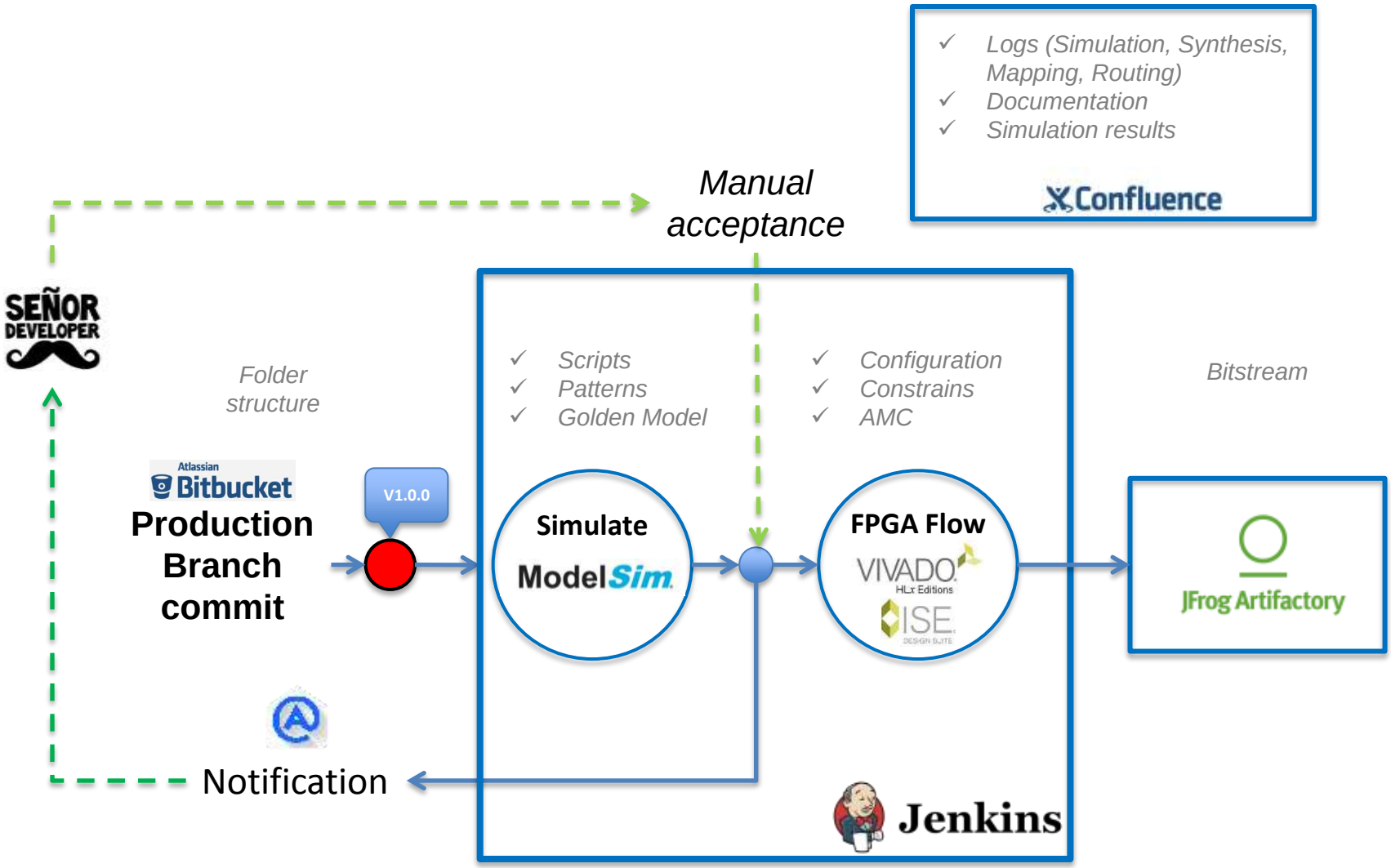
Atlassian Bitbucket



http://semver.org/

MAJOR.MINOR.PATCH

- MAJOR version when you make incompatible API changes
- MINOR version when you add functionality in a backwards-compatible manner
- PATCH version when you make backwards-compatible bug fixes


✓ Logs (Simulation, Synthesis, Mapping, Routing)
✓ Documentation
✓ Simulation results
Confluence
Manual acceptance
SEÑOR DEVELOPER
Folder structure
✓ Scripts
✓ Patterns
✓ Golden Model
✓ Configuration
✓ Constrains
✓ AMC
Bitstream
Atlassian Bitbucket
Production Branch commit
V1.0.0
Simulate
ModelSim
FPGA Flow
VIVADO HLx Editions
ISE DESIGN SUITE
JFrog Artifactory
Notification
Jenkins

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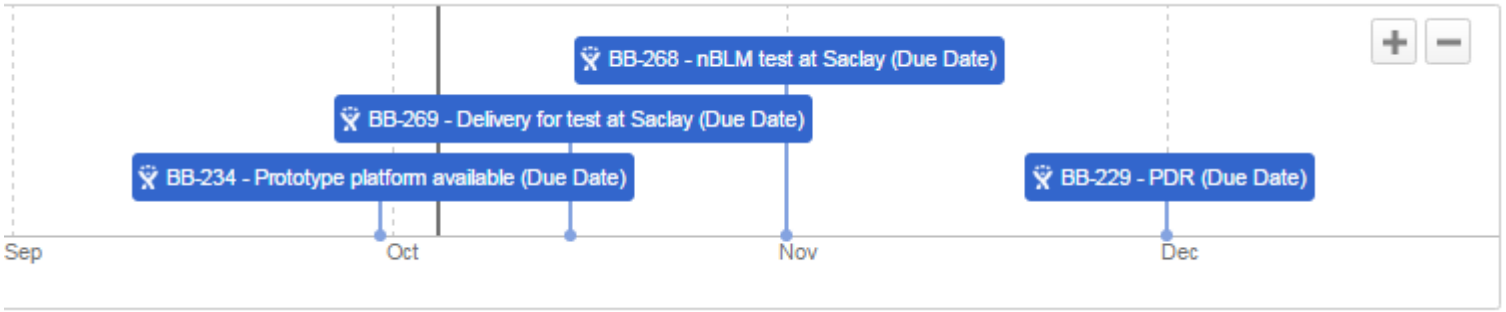
BPI page mileston

Milestones

Key	Summary	T	Due	Status	Group	Domain	Description	Affected Version/S	Linked Issues
BB-269	Delivery for test at Saclay		Oct 15, 2016 00:00	LATE	BD, ICS	PBI system	uTCA based system with DAMC-FMC25 AMC and AD9434 FMC needs to be delivered to CEA/Saclay by the 1st November 2016. Shipping is planned for 20 October 2016. Note that uTCA system can be delivered without the timing receiver due to the nature of the test.	nBLM prototype	
BB-268	nBLM test at Saclay		Nov 01, 2016 00:00	TO DO	BD, ICS, IKC	PBI system	Test with backup solution AMC and FMC at CEA/Saclay shall be performed between 1 and 15 November 2016. Test results shall be presented at PDR on 1 December 2016.	nBLM prototype	
BB-234	Prototype platform available		Sep 30, 2016 00:00	LATE	BD, ICS	PBI system	Prototype application specific PBI system development can commence.	nBLM prototype	
BB-233	CDR			TO DO	BD, ICS, IKC	PBI system	Approve the final design, start procurement of electronics hardware for installation.	nBLM final	
BB-232	Installation 1			TO DO	BD, ICS	PBI system	PBI system electronics are deployed in the gallery.	nBLM final	
BB-229	PDR		Dec 01, 2016 00:00	TO DO	BI, ICS, IKC	PBI system	Decide on further activities leading to prototype system.	nBLM prototype	



nBLM test

The ESS-nBLM-500M is a custom application develop on top of the **CAEN ELS DAMC-FMC25** carrier board. The board mounts two **Analog Devices AD9434** evaluation boards which provide one 500 MSPS, 12 bit channel each.

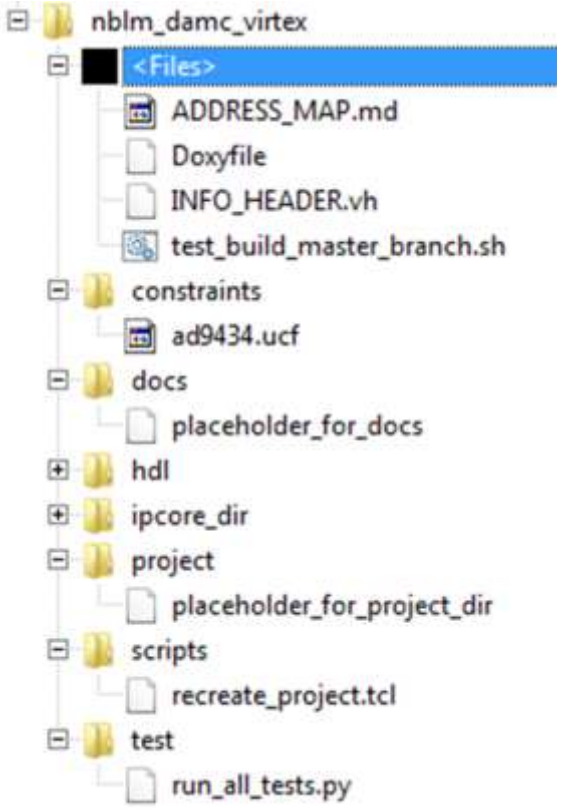
The following test equipment was used during the evaluation of ESS-nBLM-500M FPGA firmware:

- Schroff 7-slot MicroTCA.4 crate
- NAT-MCH-PHYS, NAT-MCH-RTM CPU board, NAT AC 600 Power Supply
- Operating system used: Debian GNU/Linux 8.6 (Jessie) with 3.16.0 kernel
- Tektronix AFG 3022B function generator

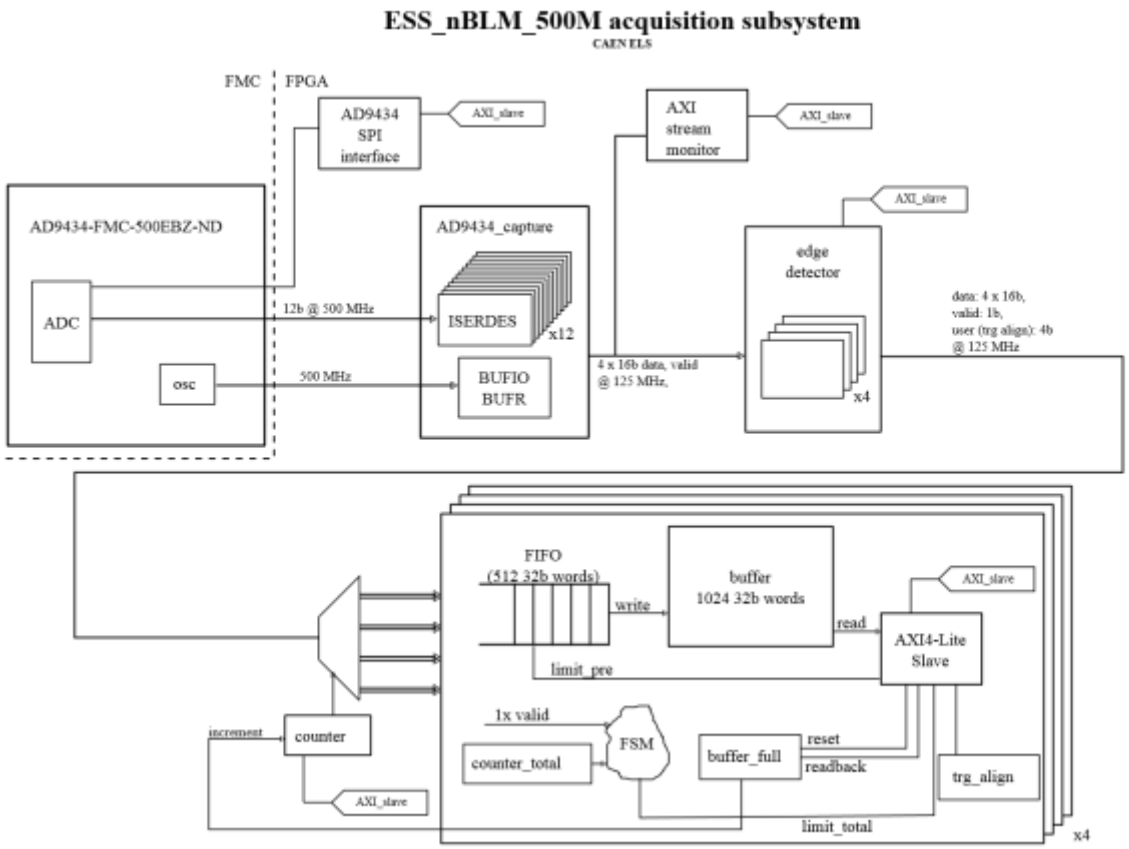
nBLM bitbucket

The used version of the FPGA firmware was 0.1.02, generated from the following commit in ESS-nBLM-500M repository (https://bitbucket.org/europeanspallationsource/ess-nblm-500m-software) with ***recreate_project.tcl*** script with **Xilinx ISE 14.7**.

The software used to perform the test was obtained from **ESS-nBLM-500M-software** repository (https://bitbucket.org/europeanspallationsource/ess-nblm-500m-software).



nBLM



This example assumes that there is a function generator attached to the input in the following configuration:

Setting	Value
Mode	Pulse
Amplitude	120 mVpp
Pulse width	30 ns
Frequency	1 kHz

The maximum event frequency was determined to be 320 Hz when capturing 1us of data (500 samples) and 270 Hz when capturing 2us of data (1000 samples).

We suspect that the limiting factor is the plotting library [SW].

Questions


Thanks!