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Control Crate

ESS raster system

DDR Control Crate
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Reference Documents

Abstract

This document contains description of the Control Crate to be used for the RSMS-PS

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1. Introduction

This document contains description for the detail design of the Control Crate to be used for the RSMS-PS.

2. Functional Description

The Control Crate is based on a standard System 8500 19” crate containing the modules shown in the block schematic next chapter.

The tasks of the control crate are:

- Central CPU module
  - Communication to local and remote control
  - Interlock Supervision
  - ON/OFF control
  - Analogue measurements
  - Mother board for regulation and DCCT module
- Signal interface module (including light guides)
- Regulation module for control of H-Bridge and DC-Link voltage according to the current set value
- DCCT interface
- Auxiliary power supplies for all electronics

2.1. Block Schematic

The figure below shows the block schematic of the control crate.

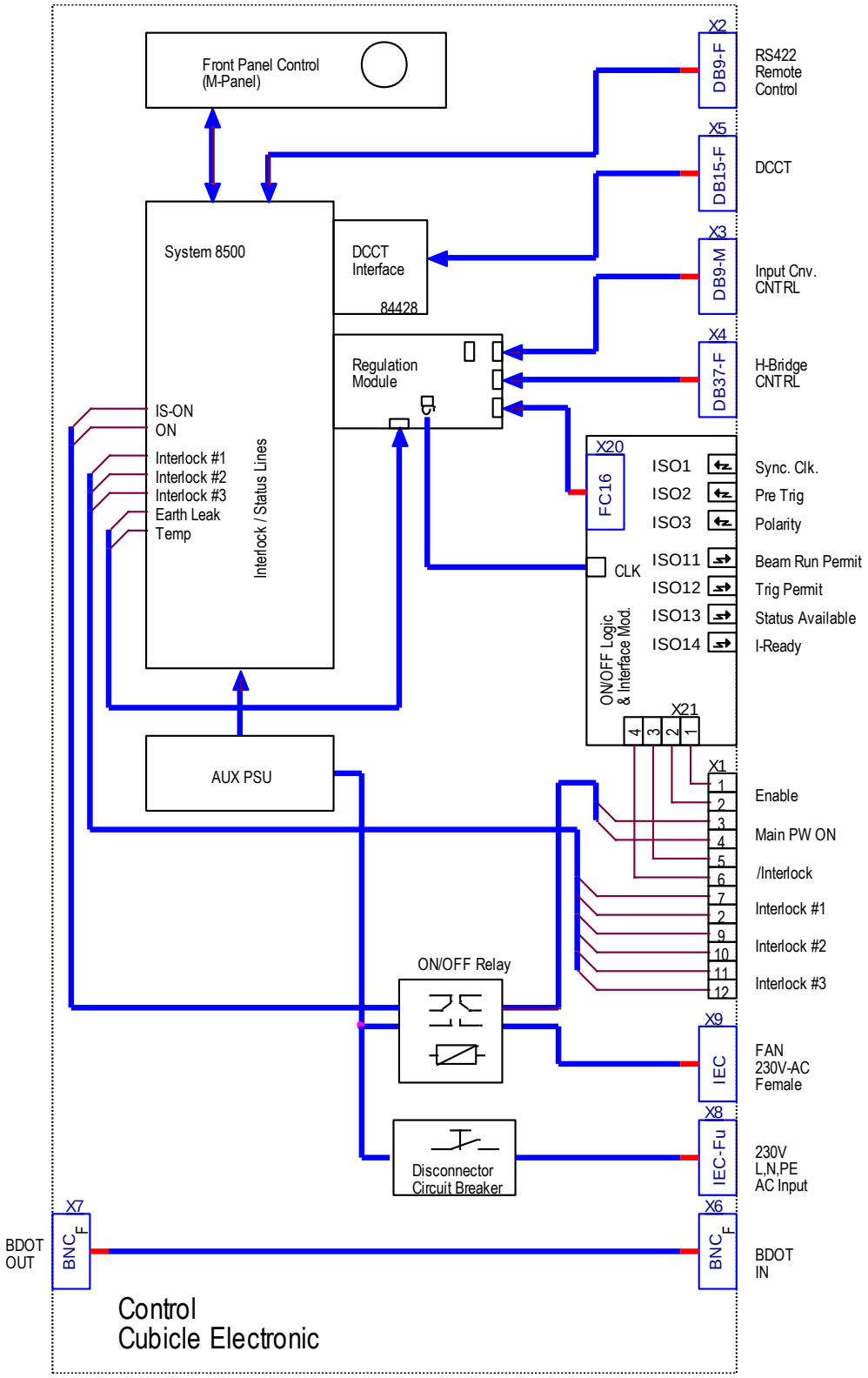

Figure 1

3. Interface

3.1. X1 Interlock Status Lines

The available interlock and status signals are connected through a Phoenix COMBICON connector with screw terminals:

12 pin Phoenix Screw Connector

Pin	Name	Value	I/O	Description
1-2	Enabled	NC	O	Normally Closed contact when PS is enabled and all OK
3-4	Main PW ON	NO	O	Normally Closed contact when PS is turned ON
5-6	/INTL	NC	O	Normally Closed contact when PS is interlock free
7-8	INTL#1	NC	I	Normally Closed Contact for interlock input 1
9-10	INTL#2	NC	I	Normally Closed Contact for interlock input 2
11-12	INTL#3	NC	I	Normally Closed Contact for interlock input 3

3.2. X2 RS 422 Remote Control

The Remote control interface signals are given in the table below. The receive line is terminated with 250Ω. The transmit line must be terminated with 250Ω at the receiver point.

DB9 pin Female connector

Pin	Name	Value	I/O	Description
1				
2	RxD-	-	I	- Receive
3	TxD-	-	O	- Transmit
4				
5	GND	-	-	Ground
6	RxD+	-	I	+ Receive
7	TxD+	-	O	+ Transmit
8	-	-	-	-
9	-	-	-	-

3.3. X3 Input Converter interface

The interface signals to the input converter are given in the table below. X3 is connected to the regulation module with a flat cable ending in an FC female connector.

DB9 pin Male connector

Pin	Name	Value	I/O	Description
1	GND		-	Return of pins 2-9
2	V_{mon_I}	(0..5V)	I	Output current monitor
3	/INHIBIT		O	Digital Inhibit signal 10k pulled up
4	V_{set_i}	(0..5V)	O	Output current set value
5	/ON	5V	O	Digital ON signal 10k pulled up
6	GND		-	Return of pins 2-9
7	V_{mon_v}	(0..5V)	I	Output voltage monitor
8	V_{set_v}	(0..5V)	O	Output voltage setting
9	V_{ref}	5.1V	I	Reference voltage

3.4. X4 H-Bridge interface

The signals to the H-Bridge in the output converter

DB37 pin Female connector

Pin	Name	Value	I/O	Description
1	AD-Power	12V	O	Power Supply Output Pin for gate driver AD
20	AD-Common		-	Common
2	AD-HS-P	5V	O	Positive Line of 5 V Differential High Side PWM Signal Pair. Terminated into 250 Ω on gate driver.
21	AD-HS-N	5V	O	Negative Line of 5 V Differential High Side PWM Signal Pair. Terminated into 250 Ω on gate driver.
3	AD-LS-P	5V	O	Positive Line of 5 V Differential Low Side PWM Signal Pair. Terminated into 250 Ω on gate driver.
22	AD-LS-N	5V	O	Negative Line of 5 V Differential Low Side PWM Signal Pair. Terminated into 250 Ω on gate driver.
4	AD-FAULT- P	5V	I	Positive Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
23	AD-FAULT- N	5V	I	Negative Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
5	AD-	5V	I	Positive Line of 5 V Temperature Dependent Resistor Output

DB37 pin Female connector

Pin	Name	Value	I/O	Description
	RTD-P			Signal Pair. Drive Strength 20 mA. Temperature Measurement is Encoded Via PWM.
24	AD-RTD-N	5V	I	Negative Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20mA. Temperature Measurement is Encoded Via PWM.
6	AD-PS-Dis	5V	O	Pull Down to Disable Power Supply. Pull Up, or Leave Floating to Enable. Gate-Source will be Connected with 10 kΩ when disabled.
25	AD-Common		-	Common
7	AD-PWM-EN	5V	O	Pull Down to Disable PWM Input Logic. Pull Up/Leave floating to enable. Gate-source will be held low through gate resistor if power supplies are enabled.
26	AD-Common		-	Common
8	AD-OC-EN	5V	O	Over-current Protection Enable. Pull down to disable detection of over-current fault. PWM and UVLO will continue to function. Pull up or leave floating to enable detection of over-current fault.
27	AD-Common		-	Common
9	BC-Power	12V	O	Power Supply Input Pin for gate driver AD
28	BC-Common		-	Common
10	BC-HS-P	5V	O	Positive Line of 5 V Differential High Side PWM Signal Pair. Terminated into 250 Ω on gate driver.
29	BC-HS-N	5V	O	Negative Line of 5 V Differential High Side PWM Signal Pair. Terminated into 250 Ω on gate driver.
11	BC-LS-P	5V	O	Positive Line of 5 V Differential Low Side PWM Signal Pair. Terminated into 250 Ω on gate driver.
30	BC-LS-N	5V	O	Negative Line of 5 V Differential Low Side PWM Signal Pair. Terminated into 250 Ω on gate driver.
12	BC-FAULT- P	5V	I	Positive Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
31	BC-FAULT- N	5V	I	Negative Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
13	BC-RTD-P	5V	I	Positive Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20 mA. Temperature Measurement is Encoded Via PWM.
32	BC-RTD-N	5V	I	Negative Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20mA. Temperature Measurement is Encoded Via PWM.

DB37 pin Female connector

Pin	Name	Value	I/O	Description
14	BC-PS-Dis	5V	O	Pull Down to Disable Power Supply. Pull Up, or Leave Floating to Enable. Gate-Source will be Connected with 10 kΩ when disabled.
33	BC-Common		-	Common
15	BC-PWM-EN	5V	O	Pull Down to Disable PWM Input Logic. Pull Up/Leave floating to enable. Gate-source will be held low through gate resistor if power supplies are enabled.
34	BC-Common		-	Common
16	BC-OC-EN	5V	O	Over-current Protection Enable. Pull down to disable detection of over-current fault. PWM and UVLO will continue to function. Pull up or leave floating to enable detection of over-current fault.
35	BC-Common		-	Common
17	Power	12V	O	Power Supply Input Pin
36	CRB-P	5V	O	Bleeder disable
18	CRB-N	0V	-	Return signal for Bleeder disable
37	OTI	NC	I	Over temperature Interlock (0V as return)
19	ELI	NC	I	Earth Leakage Interlock (0V as return)

3.5. X5 DCCT interface

The signals are connected with a DB15 Female connector on the back of the crate.

DB15 Female connector

Pin	**Name**	**Value**	**I/O**	**Description**
1	-			Not connected
2	-			Resistor to ground
3	OCP-RTN		I	Over Current / Malfunction Return
4	0V	0C		Common & screen
5	-VCC	-15V	O	Negative Power Supply
9	+Out		I	Proportional output current 1:2000
10	-			Not connected
11	OCP		I	Over Current / Malfunction
12	+VCC	+15V	O	Positive Power Supply

Non used pins are not connected

3.6. X6 & X7 B-Dot

One female BNC plug for B-Dot input located at the back –X6
One female BNC plug for B-Dot output located on the front –X7

3.7. X8 Line Input

Main power to the control crate is passed through an IEC plug.

3.8. X9 Fan Power

The fan power to the output converter is passed through a female IEC plug.
Protection is ensured by the disconnector / circuit breaker in the control crate.

3.9. ISO1 to ISO15 Optical Control

Pulse raster control is performed through light guides. The light guides are connected directly the transmitter or receiver located on the back of the crate. The light guide chips are shown below.

Light guides

Plug	Name	I/O	Type	Description
ISO1	Sync. Clk.	I	HFBR-X4XX	External Synchronization Clock 88 MHz
ISO2	Pre-Trig	I	HFBR-X4XX	Pre-trig signal telling PS to start a pulse burst
ISO3	Polarity	I	HFBR-X5XX	Sets the starting pulse polarity
ISO11	Beam Run Permit	O	HFBR-X4XX	Beam may be issued
ISO12	Trig Permit	O	HFBR-X4XX	PS ready to start a pulse burst
ISO13	Status	O	HFBR-X5XX	Status available on serial line
ISO14	I-Ready	O	HFBR-X5XX	Output current for last burst was within 1% of set value
ISO15	Missing CLK	O	HFBR-X5XX	External clock is missing

HFBR-14xxZ and HFBR-24xxZ Series
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Data Sheet

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4. Sub Modules

Below is a short description of the modules used.

4.1. Central CPU Module

For the central control the standard System 8500 Control Module is foreseen with following change notes:

- The latched /Interlock signal must be strapped to pin P2-A9 (Regulation module connector).

Please see manual for the System 8500 control module for deeper description.

4.2. DCCT Interface

The DCCT Interface module is a small PCB supplying the voltage supplies to the DCCT and to pass the measured current to the right pins to the system 8500 module.

4.3. Regulation Module

The regulation module is described in a separate document. Please refer to this for further information.

4.4. Fibre Optic Interface Module

The Signal Interface module is where the external Fibre optic are connected. Its task is to receive, convert and pass the signals to/from the regulation module.

4.5. ON / OFF Relay

The ON/OFF relay is activated when the power supply is turned ON. When ON then:

- Tells the control CPU that it is ON, thereby also enabling the HV capacitor charger.
- Delivers 230V for the fans.
- Delivers a closed contact to the user telling that the RSMS-PS is ON.

4.6. M-Panel

Standard System 8500 M-Panel Module with following change notes:

- Voltage and currents setting/read back set to units

4.7. Aux PSU

Standard System 8500 Aux PSU Module

4.8. 230V AC FAN Power

A 230V AC line power is passed to the output converter through an IEC female plug.

4.9. Circuit Breaker

The 4A manual operated circuit breaker is accessible from the front panel.

4.10. B-Dot

The magnet delivers a B-Dot signal which is passed from the input connector X6 to the output connector X7 without any modification.

The output must always be terminated by a 50Ω resistor.

For a deeper description of the B-Dot signal please refer to the document "502446 DDR-RSMS-PSU RevA.docx" describing the overall system.

5. Mechanic Design

The Control Crate is built in a 19" rack system having following dimension:

- With: 19"
- Height: 3U
- Depth: 650mm

5.1. Mechanical Drawings

Figure 2

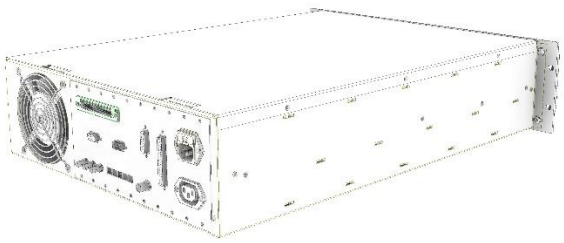

Figure 3