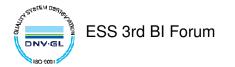


Elettra Sincrotrone Trieste





AFE and BE development upgrade

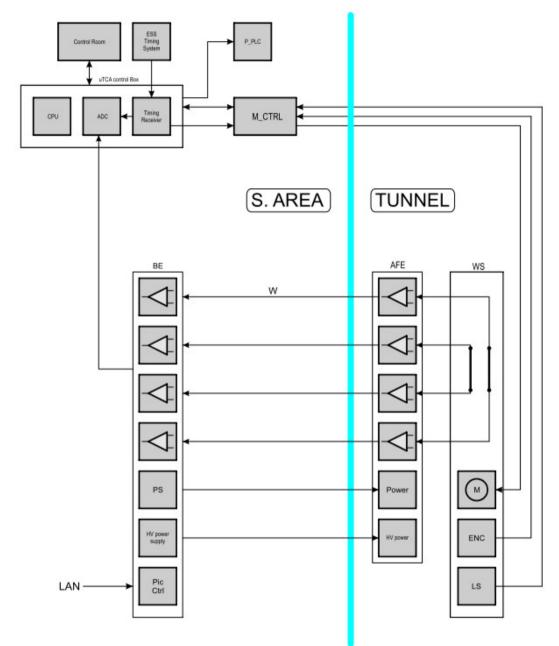


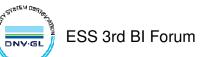




WSAS simplified system block diagram Diagram by S.Grulja







180 900

3

JSTEM M

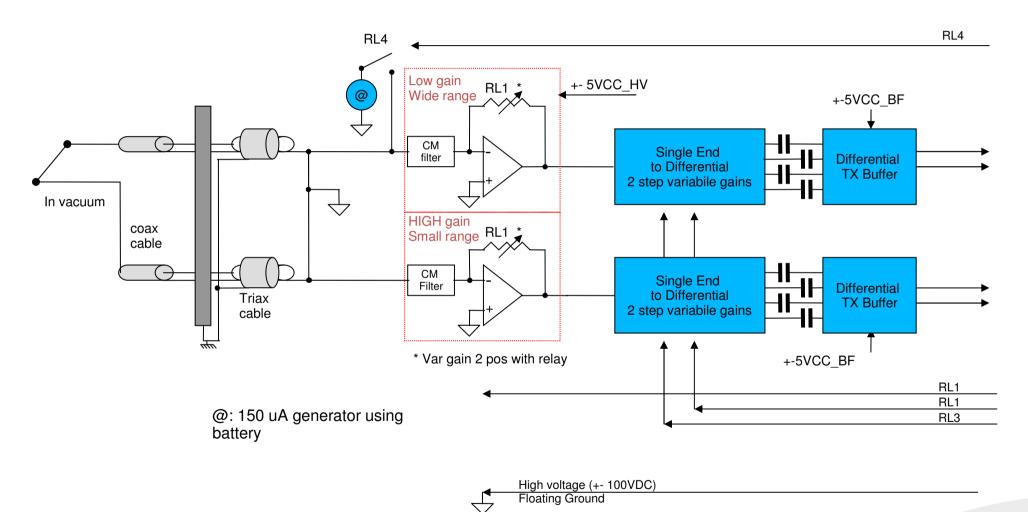
DNV·GL

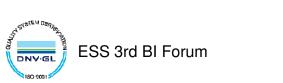


Simplified Block Diagram for AFE V1.0



Analog Front End TWO IDENTICAL STAGES: Horizontal and Vertical



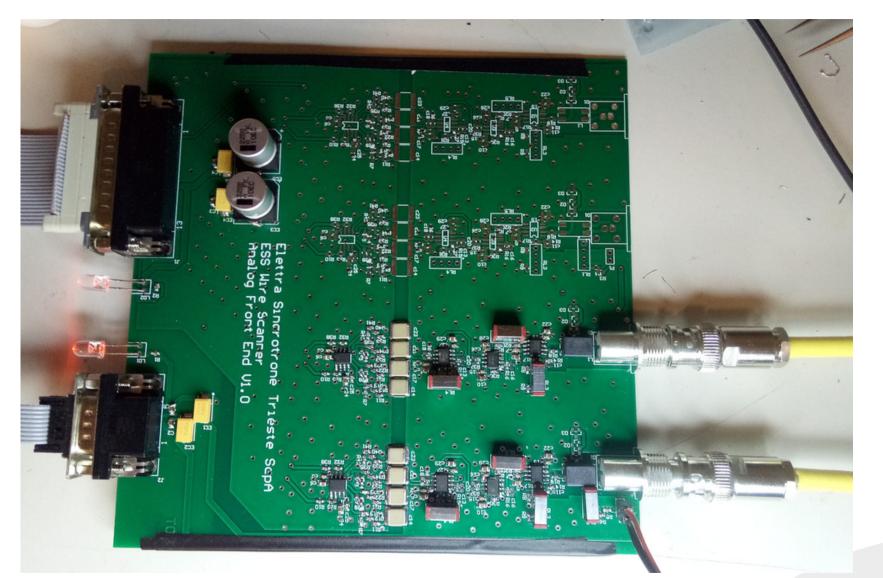


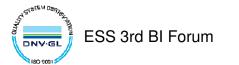
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AFE prototype







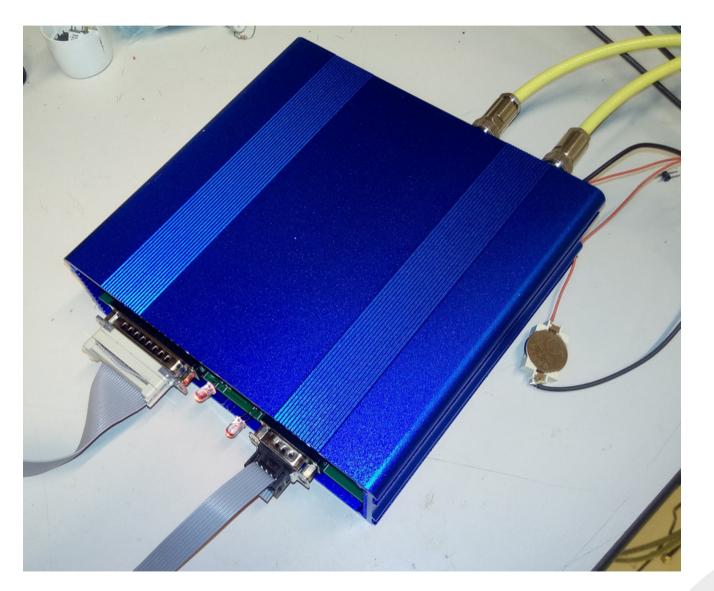


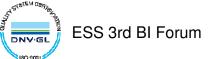
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WS Analog Front-End BOX









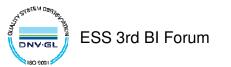




AFE specifications



Parameter	Value	Symbol	Notes		
Input channel	4	I_Wi; i=14	Tri-axial		
Max Input Voltage	3VAC	I_W _{MAX}	Input diode protected		
Max Input Current	N/A	I_W _{MIN}			
Input Impedance	50 ohm	Z _{IN}	Not well matched		
Bandwidth	2MHz	BW _{AFE}			
Output channel	4	OUT _{AFE} i	Balanced twisted pair		
Minimum Gain	1V/400μA	G _{MIN}	V / A		
Maximum Gain	1V/1μA	G _{MAX}	V / A		
Power supply	+/- 5 V @ 50mA MAX	I _{supply}	via BE cable		
Dimension	170 x 160 x 54		mm		
Weight	400 g				



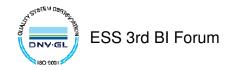
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SYSTEM ON

DNVGL



- The input signal range has been extended by adding two relays in the signal chain. It also increase the gain of the entire system.
- Added a Common Mode Choke to filter better the input signal. It prevent also some parasitic charges to interfere with the signals.
- Added a strong capacitor (2200uF) on the Buffer power supply to increase the output buffer performances.

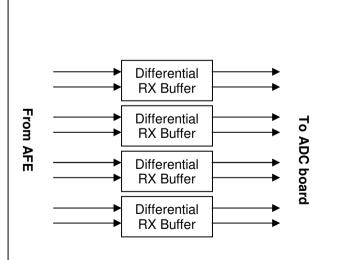








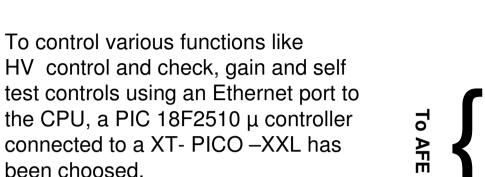
OHEAS LACCT 9

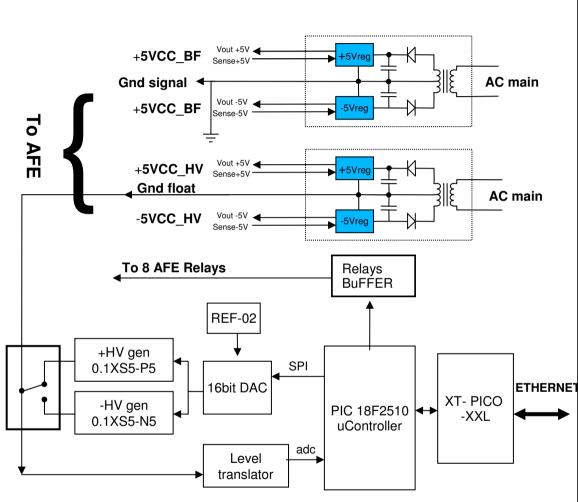


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Trieste

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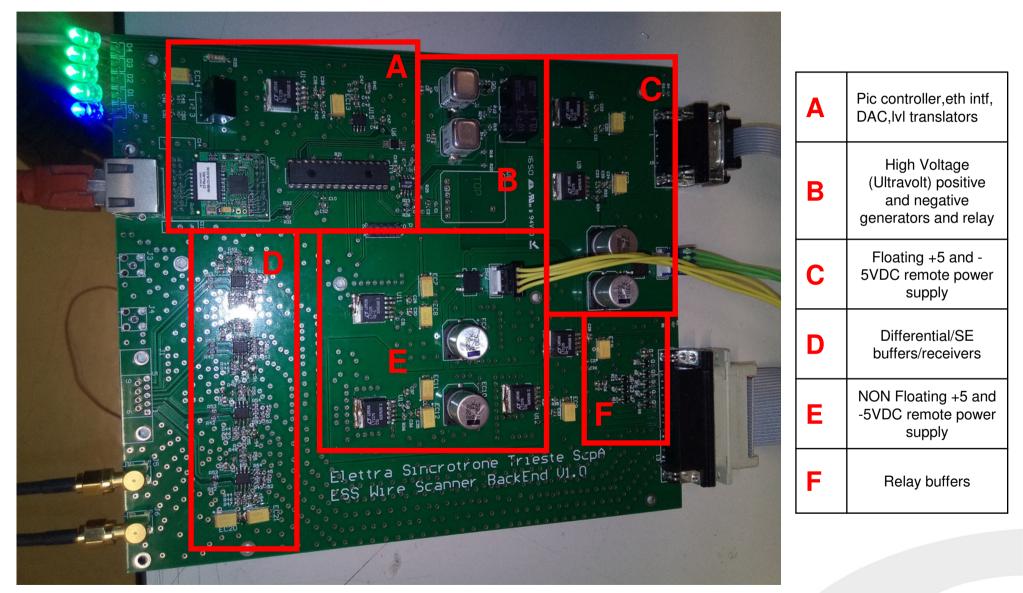


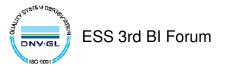




BackEnd in practice







Raffaele De Monte, Apr 27, 2017







Input /outputs:

- 1 x DB9 : +-5VDC Floating power supply
- 1 x DB25: +-5VDC NON floating P.S., 8 relays outputs, 4 differential signal inputs
- 2 x 4pin header: 2x6.3VAC inputs (transformers)
- 4 x SMA: Low impedance S.E. signal analog outputs
- 1 x DB9: Low impedance differential signal analog outputs
- 1 x RJ45: Ethernet communication port
- 1 x 5+5 header: PIC programming connector
- 1 x Blue LED: uController activity
- 4 x Green Led: +5V/-5Vfloat, +5V/-5Vnonfloat power return from AFE (off if AFE not connected)



11





Simple command protocol:

All commands are in ASCII format with Carriage Return (cr) character termination ALL unrecognized commands return 'KOcr'

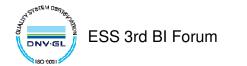
SET FUNCTIONS: all of the 'SET' commands return 'OK' string or 'KO' if wrong parameter

SetVoltage: (integer) Sets the bias voltage: the command starts a *procedure* that sets the DAC <u>until</u> the desired value is reached: the DAC has to be set in +- 10% of the theoretical set value. If > of 10% a error flag is set.

SV:voltage (from -100 to +200)

SetBit (8BIT 0-255) : sets the 8 bits that controls gain and test input current SB:number

Set Pulse for wire test (time): Sets all of the relays in a condition to read the reference current for a limited time expressed in microseconds, then revert all back **SP:number**



Raffaele De Monte, Apr 27, 2017







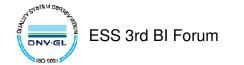
READ FUNCTIONS: all of the 'Read' commands returns ascci value terminated by a CR

```
Read Voltage (returns from -100 to +200) RV?
```

```
Read Bits (returns 0-255) RB?
```

```
READ TEMPERATURE (returns da 0 a 100) Only for SCINT version RT?
```

```
READ STATUS: it returns a string:
SETVOLTAGE:READVOLTAGE:BITS:SWVERSION:SWTYPE:RMF:COUNTER
where:
SWVERSION : number 1 - 0xFFFF
SWTYPE : 1 = WS 5=SCINT
RMF : 'R' if Running, 'M' if Moving, 'F' if Fault
COUNTER : loop counter (WATCHDOG purpose)
RS?
```

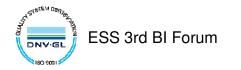


DHEAS 180





- 0.5A 3.3V DC-DC converter (powering Ethernet interface) vulnerability : solved changing with a 1A version
- Ripple noise in HV (~200mV pkpk ~10KHz): solved adding HV capacitor (4.7uF 250VDC)
- Buffer Power supply (on +5VDC) fail on power up due to shifting on negative at power off because of high capacitors: solved adding resistors to discharge fast and equally the capacitors.
- Poor precision in high voltage generator: a readback/set function has been implemented in the PIC software to reach the desired value with a single command. An asyncronous system has been implemented.
- The output signal is monopolar 0-5V. The ADC from Struck board accept +-1VDC. Solved putting a 50ohm attenuator (loosing 1 of the 16 bits..)







WS Wire Integrity Check



Command SENT via ethernet: SP:1500

Agilent Technologies MON APR 24 09:44:39 2017									39 2017
1 500 % /	2 2.00V/	′ <mark>3</mark>	4	\rightarrow	8.200	500.0%	/ Trig'd?	<u></u>	556 0
					r				
¥ <u></u>									
_									
2									
Edge Trigger	Menu								
Source		Slope	1						
2		f							

Result with intact wire

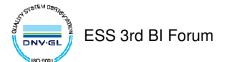
 Agilent Technologies
 MON APR 24 09:45:37 2017

 50007/
 2.00V/
 2.00V/
 2.00V/
 33.37

 Image: Constraint of the straint of t

Result with broken wire

Set Pulse for wire test (time): Sets all of the relays in a condition to read the reference current for a limited time expressed in microseconds, then revert all back





Conclusions



- The Back End prototype PCB has been implemented
- The full functionality of the Back End has been tested
- The full functionality of the Back End connected to te Front End has been tested
- The firmware for the PIC uController is running in 'beta' version
- The system is ready to be connected to the uTCA acquisition crate





"Funny" Triaxial connectors





Specify if **<u>2</u> or <u>3</u> lug !**









<mark>Elettra</mark> Sincrotrone Trieste

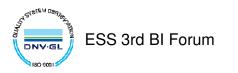


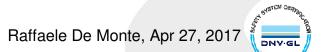
www.elettra.eu



SPARE SLIDES





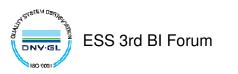


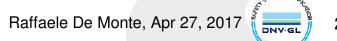
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WSAS simplified system laboratory test bench







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