Low Level Radio Frequency System (LLRF) of the RFQ for MYRRHA

On behalf of MYRTE LLRF Team

MYRTE project has received funding from the EURATOM research and training program 2014-2018 under grant agreement N°662186*)*

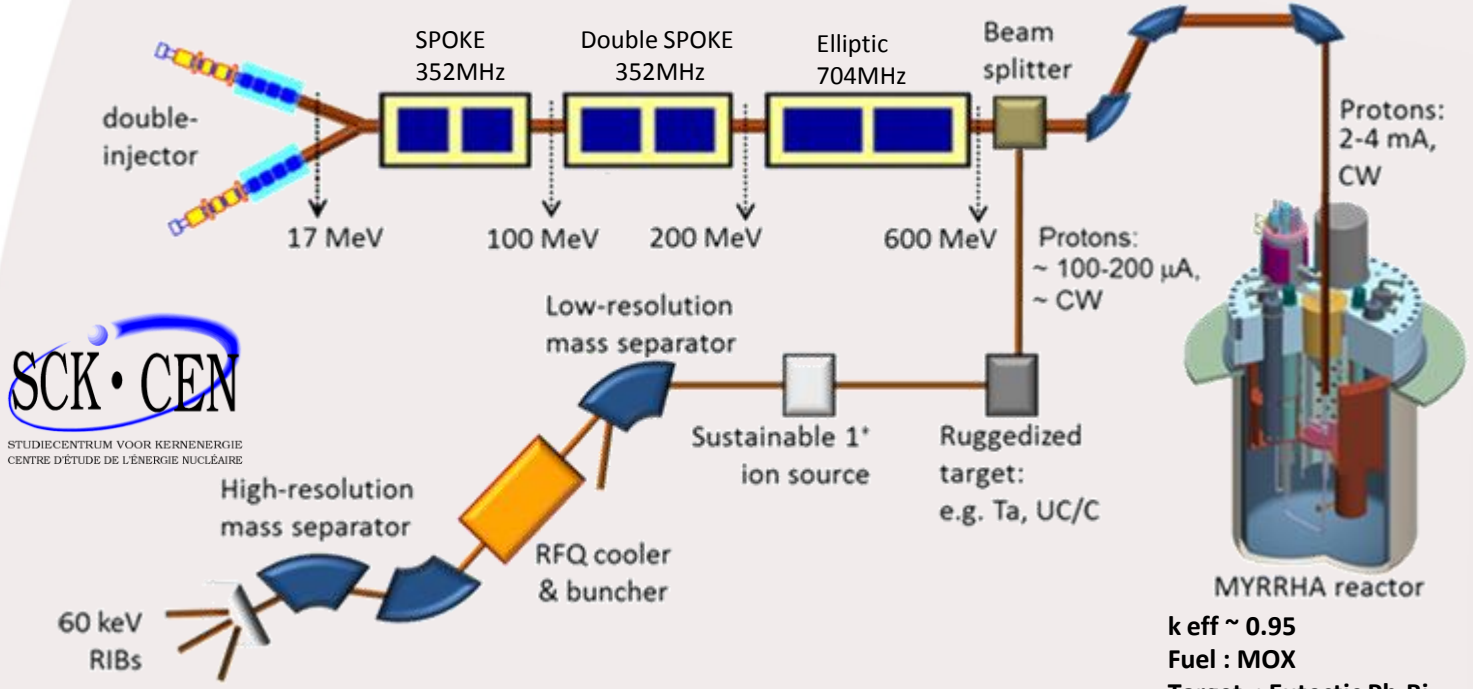
SLHiPP-7 – ORSAY – 8th June 2017

Outline

- MYRRHA Context
- Specifications for LLRF
- LLRF system overview
- Status

MYRRHA context

Multi-purpose hYbrid Research Reactor for High-tech Applications



SCK • CEN
STUDIECENTRUM VOOR KERNENERGIE
CENTRE D'ÉTUDE DE L'ÉNERGIE NUCLÉAIRE

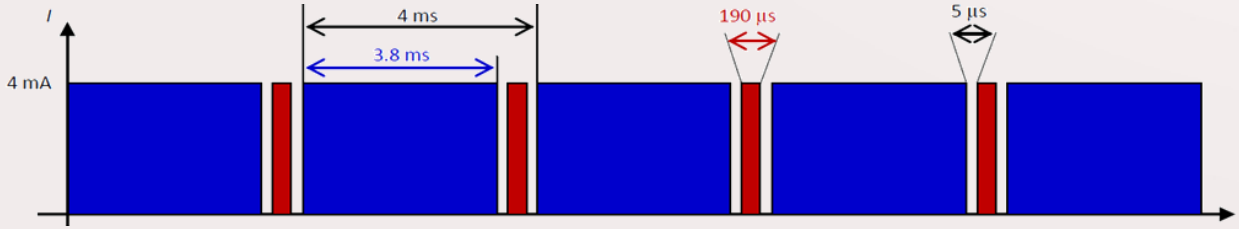
k eff ~ 0.95
Fuel : MOX
Target : Eutectic Pb-Bi
Reactor :
-Subcritical (65-100MWth)
-Critical (100MWth)

Goals :

- To build a hybrid reactor demonstrator for transmuting radiotoxic waste, (ADS).
- To product Radio Isotopes to medicine
- For fundamental research

MYRRHA context

CW RF with pulsed beam



→ **High power proton beam (up to 2.4 MW)**

Proton energy	600 MeV
Peak beam current	0.1 to 4.0 mA
Repetition rate	1 to 250 Hz
Beam duty cycle	10^{-4} to 1
Beam power stability	< ± 2% on a time scale of 100ms
Beam footprint on reactor window	Circular ∅85mm
Beam footprint stability	< ± 10% on a time scale of 1s
# of allowed beam trips on reactor longer than 3 sec	10 maximum per 3-month operation period
# of allowed beam trips on reactor longer than 0.1 sec	100 maximum per day
# of allowed beam trips on reactor shorter than 0.1 sec	unlimited

→ **Extreme reliability level**

MYRRHA context

MYRRHA Research and Transmutation Endeavour (MYRTE) :

The goal of MYRTE, a H2020 European project is to perform research to support the development of the MYRRHA facility during 4 years (may2015- may2019) with a main topic , the Injector demonstration within the framework of the WP2 :

WP2 : Accelerator R&D for ADS/MYRRHA

D2.1 Realisation of a full-size MYRRHA-type RFQ demonstrator (IAP) (M30)
D2.2 Construction of a prototype Solid State RF power amplifier (IBA) (M30)
D2.3 Digital LLRF development (CNRS) (M30)
D2.4 Beam diagnostics development (CEA) (M48)
D2.5 Control system development in a highly reliable accelerator context (COSYLAB) (M48)
D2.6 Beam simulation code development, global coherence (CEA) (M48)
D2.7 Injector commissioning (SCK•CEN) (M48)
D2.8 Space-charge experiments (CNRS) (M30)
D2.9 LINAC4 reliability analysis (CERN) (M48)
D2.10 MYRRHA SRF spoke R&D (CNRS) (M30)
D2.11 SRF CH demonstration with beam (IAP) (M30)
D2.12 MYRRHA linac cost estimation (SCK•CEN) (M18)

Specifications and Constraints

RFQ

Length : 4 m
Frequency : 176.1MHz
Bandwidth : 83.8 kHz
Nominal power : 108kW
Commissioning : Pulsed with duty cycle =1% min to CW

LLRF budget :

Amplitude stability : +/-0.2% rms
Phase stability : +/-0.2° rms

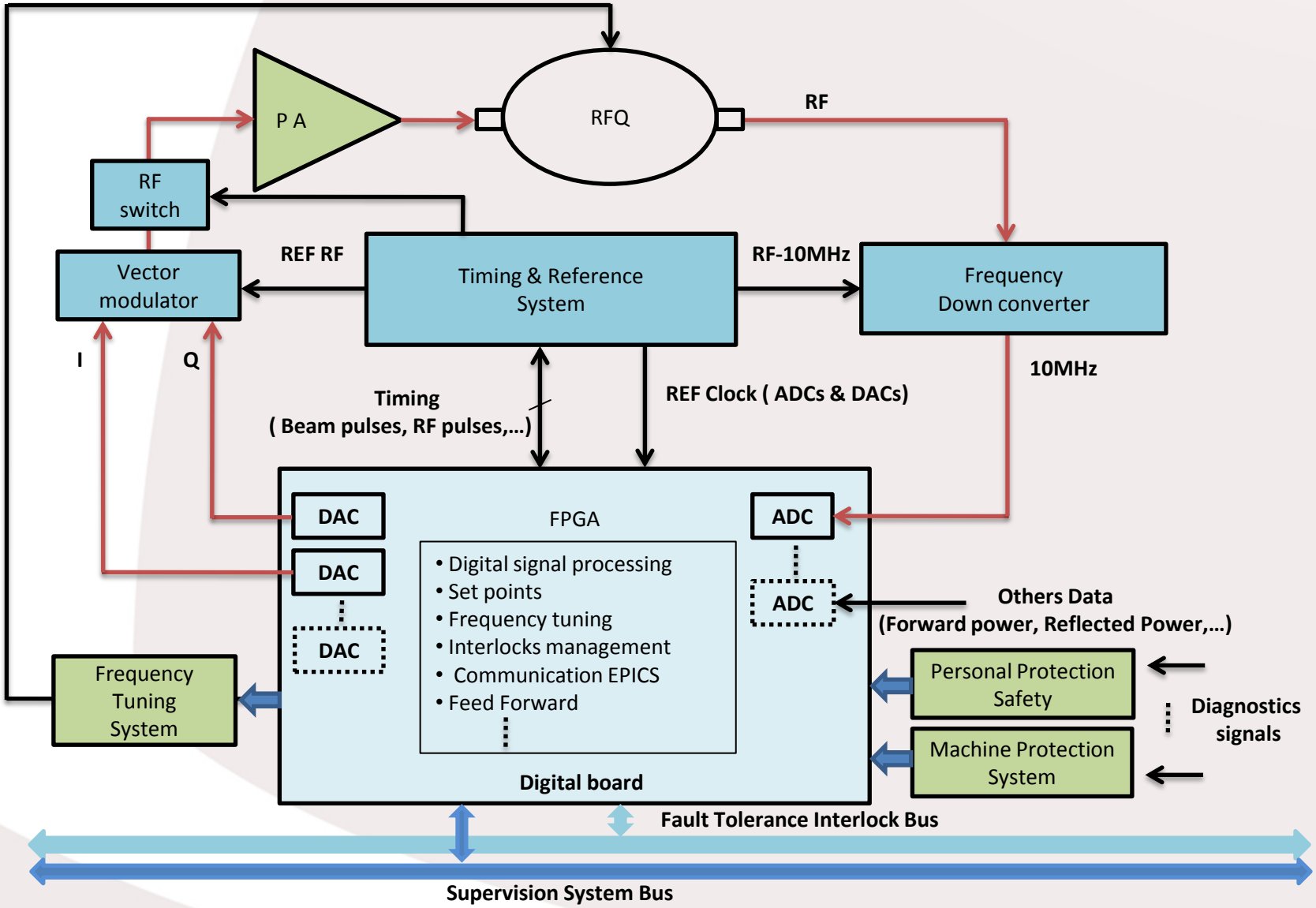
budget error to share between 3 parts :
-the Phase Reference Generation System
-the Phase Reference Distribution System
-the A&P feedback system
→ Worst case : +/-0.1% rms and +/-0.1° rms each

LLRF and Phase references generation systems

Duration : 2.5 years with ~ 1.5 FTE/ year

Interfaces with a lots of systems as Machine Protection System (MPS), Safety Protection System (SPS) , RF Power Amplifier (RF SSPA) , Frequency Tuning System (FTS),...

LLRF Basic Scheme



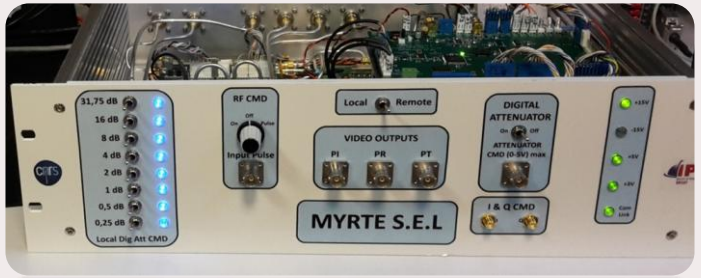
LLRF prototype Choices

To re-use RF developments :

- Down converter system (352MHz to 10MHz) developed within the framework of a LLRF R&D with the PXI standard. The adaptation to 176.1MHz to 10MHz is limiting due to a PCB using components with the same footprints in the frequency range 88,05MHz to 704.4MHz.

→Intermediate Frequency signal is not ideal for limiting the latency but easy to obtain in the case of a test bench.
(output available in rear of RF synthesizer)

- Analog Self Exciting Loop used for testing superconducting cavities with an adaptation to synchronize the RF with the Phase reference signal.



→ More hardware than digital SEL (of course) but it's operating with more 50dB dynamic.

Courtesy S. Berthelot

LLRF prototype Choices

To re-use RF developments :
-Phase References Generation System

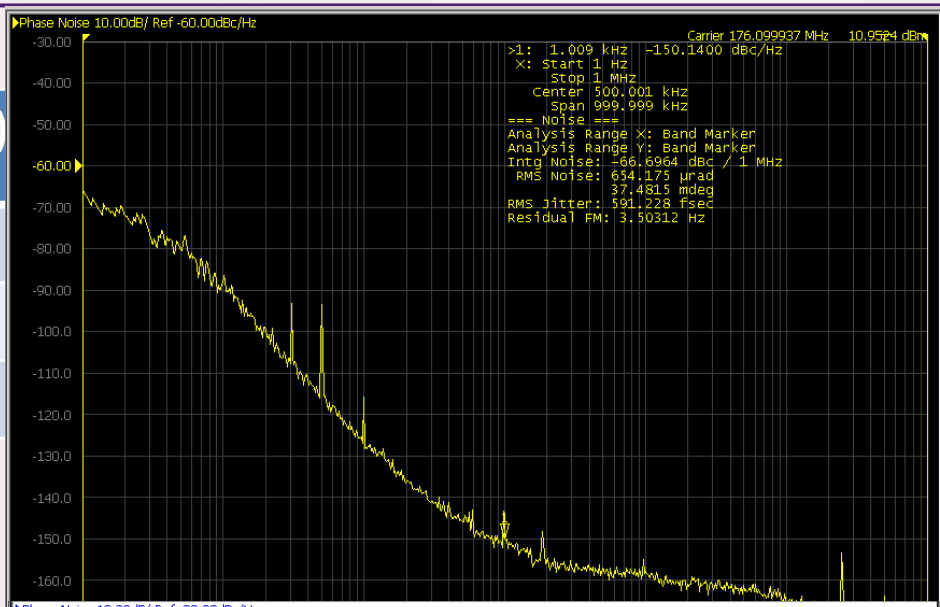
LLRF prototype Choices

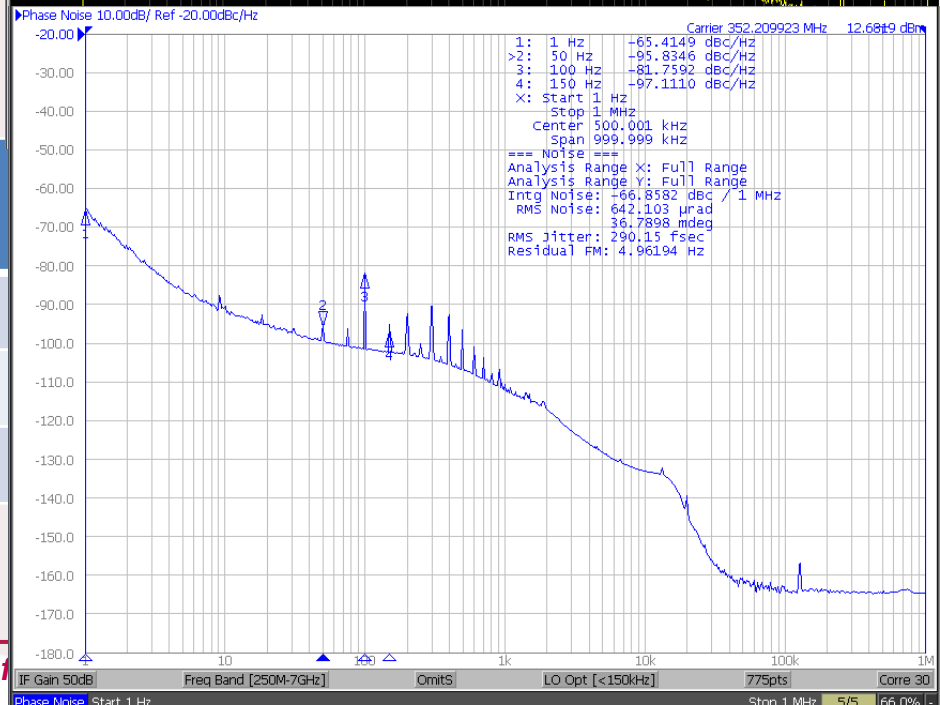
Frequency (MHz)	Jitter rms (°)	Noise Phase (fs) (1Hz-1MHz band)
176.1	0.037	591
352.2	0.082	651
704.4	0.170	670

Test with SML03 synthesizer
Instead of the 88.05MHz PLL
+ filter

Frequency (MHz)	Jitter rms (°)	Noise Phase (fs) (1Hz-1MHz band)
176.1	0.018	288
352.2	0.037	290
704.4	0.072	285

→New PLL bought but not still implemented



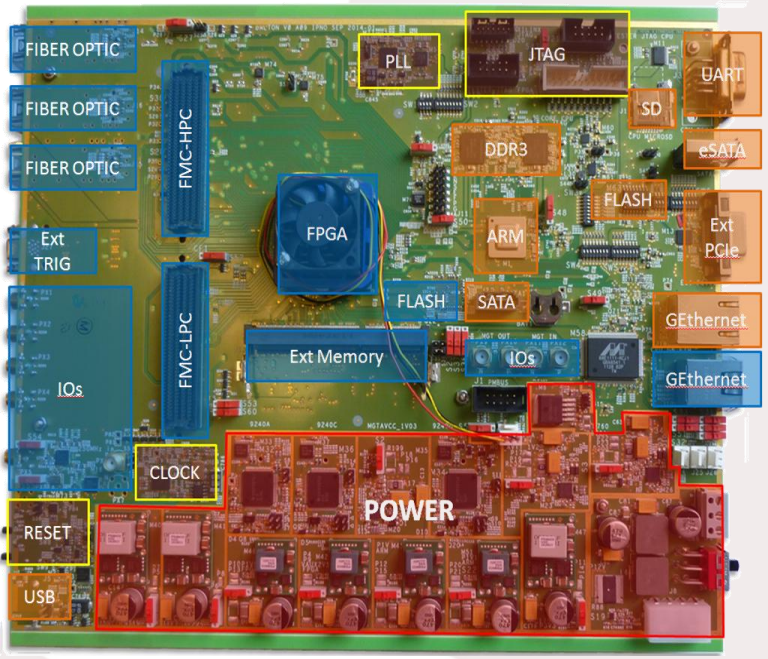


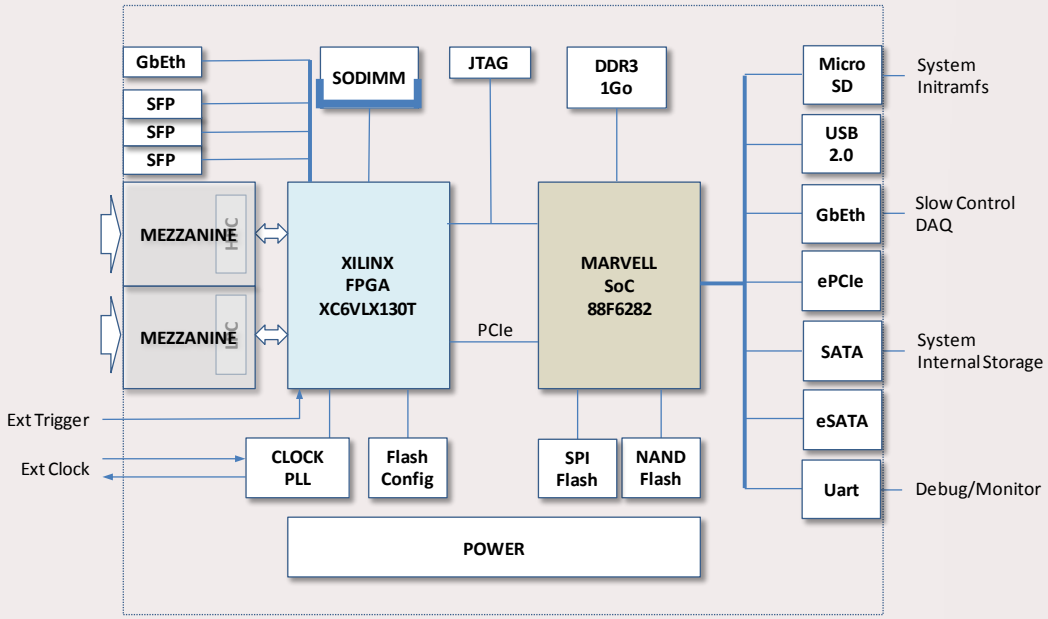
LLRF prototype Choices

To re-use :

- An in-house Digital board (DALTON) using a XILINX FPGA associated to a ARM processor with a PCIe link. Also less software developments (driver PCIe Ok) like an Off-the-shelf solution

Digital Mother Board developed at IPNO
(courtesy Beng-Yun Ky)



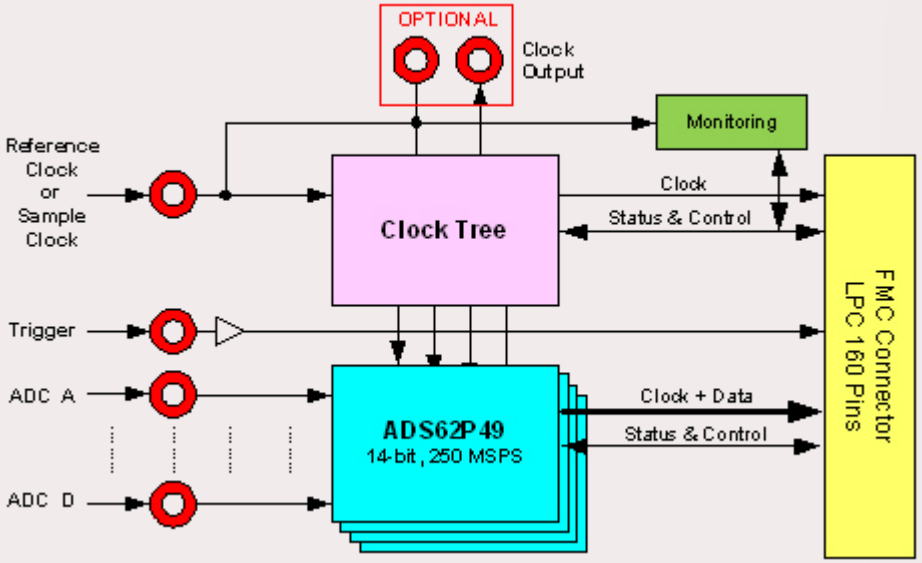


Debian 8 « Jessie » implemented with an SATA hard disk
(Scientific Linux won't work for ARM based architecture)

LLRF prototype Choices

To use :

- ADC mezzanine FMC board Off-The- Shelf form 4DSP (FMC104) : 4 channels

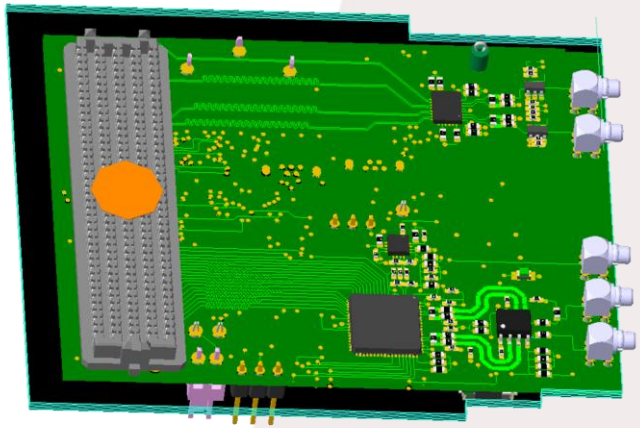


→ Low Pin Count (LPC 160 pins) compatible but in this case, Clock tree and ADC configurations are not possible! In fact it's a FMC108 without some front-end components then operating also on a HPC slot (400 pins)

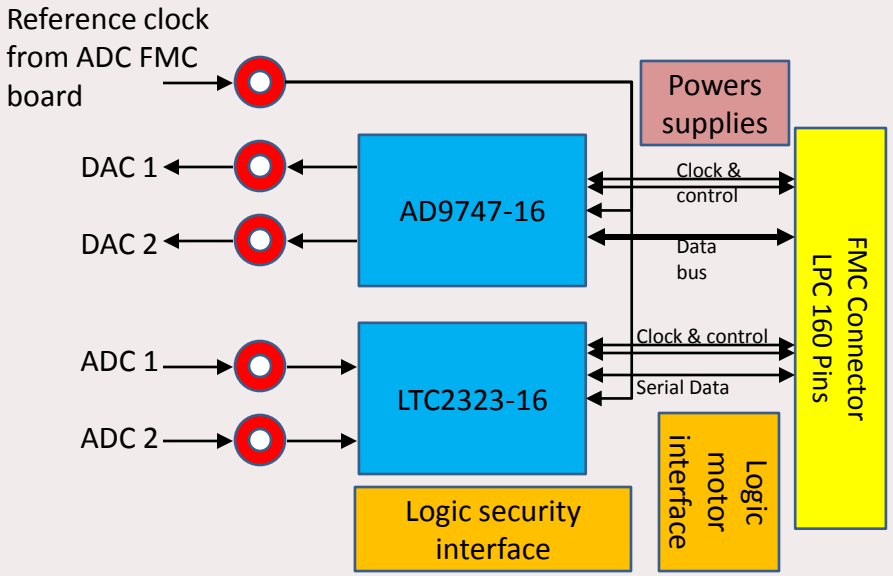
LLRF prototype Choices

To develop :

- DAC&AUX mezzanine FMC board prototype



Courtesy J-F. Yaniche



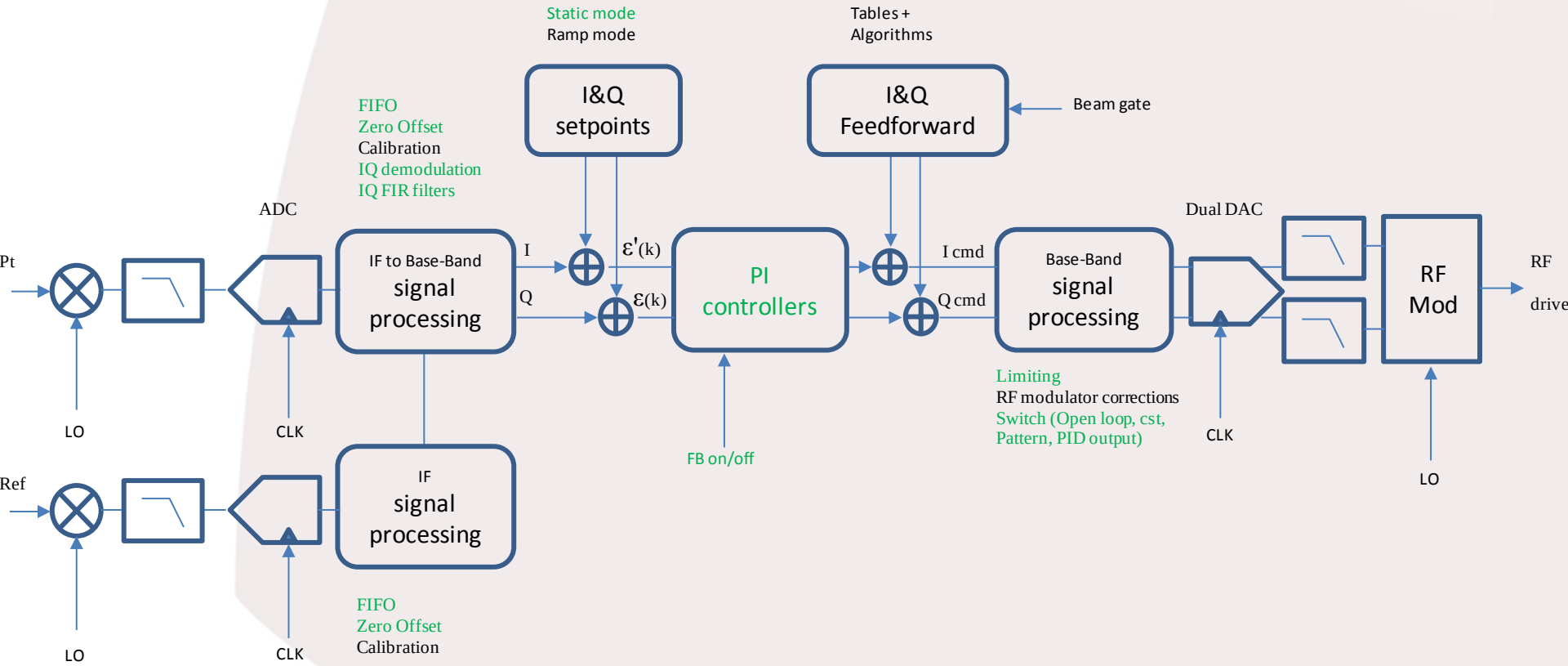
→ Low Pin Count (LPC 160 pins) only but many interfaces connectors implying micro connectors, 8 layers with differential lines, controlled impedance 50 Ohm and 100 Ohm on the same layer, ...

→ Order for PCB passed

VHDL for LLRF system

To develop :

- VHDL software : Main loop example

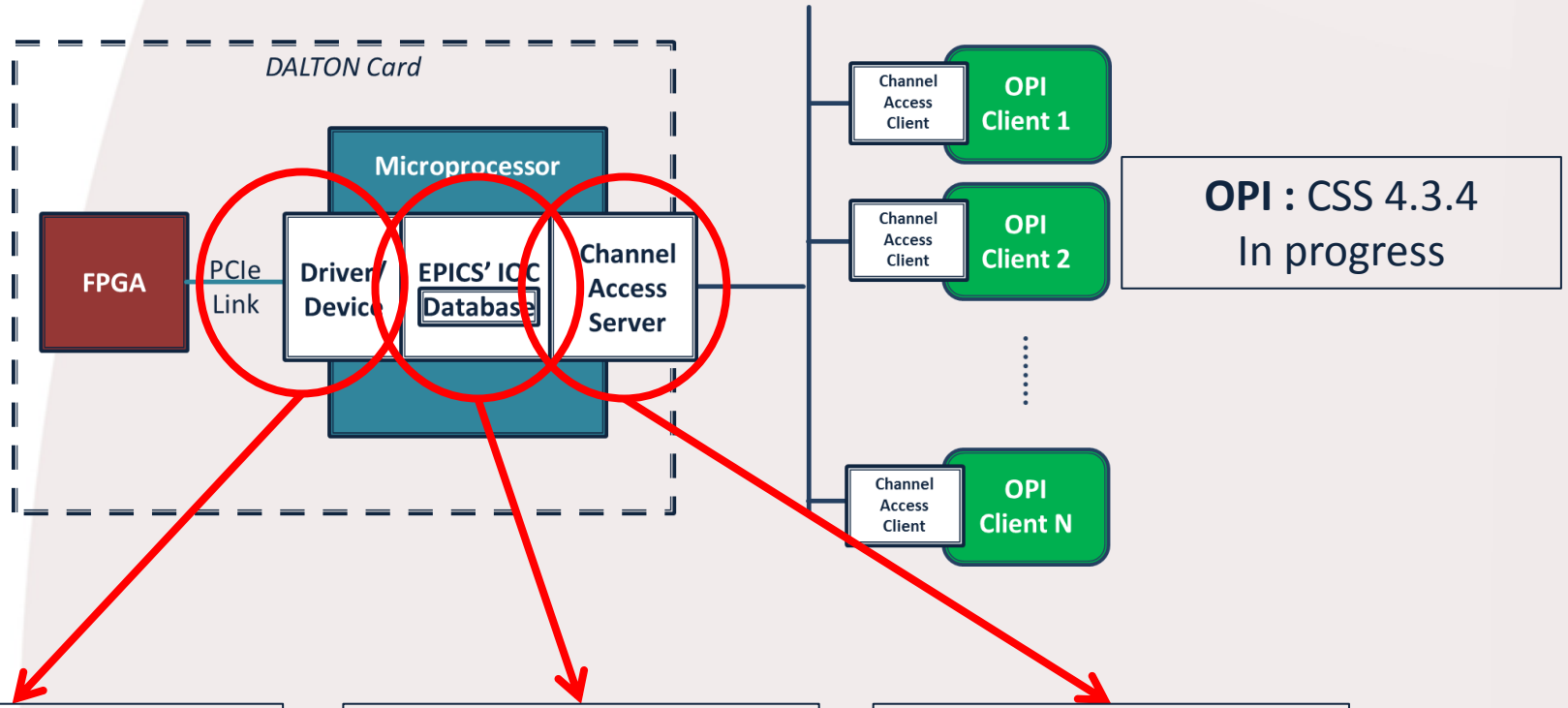


→ Code in progress with a important part about registers access with the communication protocol

Courtesy T. Le Ster

EPICS for the LLRF system

Courtesy W. Sarlin



Summary

Actual tasks in progress

- VHDL Code : ADC configuration, ADC readout, IQ demodulation, PID done but still a lot of work .
- System Integration : close to the end
- EPICS : records processing and OPI in progress

Goals

- Tests of the whole system with our test bench in September
- Digital Self Exciting Loop development

→ In parallel, we are progressing about a MTCA version using a major part of the LLRF prototype features within the framework of MYRRHA R&D 100MeV

Thank you for your attention