Master Oscillator for ESS

Design description

Version 1.0

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1. Version history

Version	Name and date	Comment
0.91	Anders Svensson, 2015-07-07	Internal draft
0.92	Anders Svensson, 2016-11-05	Electrical updates
0.93	Anders Svensson, 2017-04-19	EVG interface changed to; 88 MHz, 1 PPS and UTC
1.0	Anders Svensson, Anders J Johansson, 2017-04-26	Updates for PDR

Table of Contents

2. Introduction

2.1 Purpose of the document

This document describes functionality and design of the Master Oscillator which is the primary clock and frequency source for ESS.

2.2 Definitions

Abbreviation	Explanation of abbreviation
COTS	Commercial Of The Shelf
DC	Directed Current
DR	Dielectric Resonator
DRO	Dielectric Resonator Oscillator
ESS	European Spallation Source
EVG	Event Timing Generator
FPGA	Field Programmable Gate Array
GPS	Global Positioning System
OCXO	Owen Controlled Crystal Oscillator
PLL	Phase Locked Loop
PPB	Parts Per Billion
LINAC	Linear Accelerator
MO	Master Oscillator
PPS	Pulse Per Second (not to be mixed up with Personal Protection System)
Rb	Rubidium
RTC	Real Time Clock
UTC	Universal Time clock
VCO	Voltage Controlled Oscillator

2.3 References

[1] EndRun Meridian GPS receiver, User manual, 2012 revision 18, EndRun Technologies

[2] Timing Generator – Master oscillator time synchronization interface, MOTG_A&D_v1 rev 0.2, 2014-11-20, ESS

[x] Xxx

3. System characteristics

3.1 System purpose

The master oscillator is the primary time and frequency source for ESS. It will provide RF frequencies to the LINAC and accurate timing for the whole ESS timing infrastructure. All signals will be generated from one common oscillator and thus all will be phase locked to each other. In order to facilitate this, the pulse frequency of the accelerator will not be exactly 14 Hz, but instead 88.0525 MHz divided by 6289464 giving 14.000000636 Hz. This way there will always be the same integer number of RF cycles in the accelerator between each pulse start. The target wheel is synchronized to the timing system and MO.

The Master Oscillator provides:

- Accurate timing information to the ESS timing system based on 88.0525 MHz clock, 1 PPS and UTC information from GPS
- Very stable phase reference signals at 704.42 MHz and 352.21 MHz for distribution by the phase reference line

Client devices having less strict jitter requirements will get timing information from the timing generator instead of MO for cost effective reasons. Timing information will be distributed over fiber cables to local timing receivers. For even lower timing requirements NTP can be used.

3.2 System overview

The MO will be locked to a GPS disciplined rubidium source to limit the drift on long time scales if the GPS is out of synchronization. To reduce the short term drift a phase locked loop (PLL) with an OCXO is locked to the rubidium source. To further reduce the phase noise the highest frequencies to be distributed 704.42 MHz, is generated with a dielectric resonator oscillator (DRO), which is phase locked to the OCXO PLL. The other frequencies needed, 352.21 MHz and 88.0525MHz, are generated by frequency division of the 704.42 MHz signal.

The MO main building blocks and high level external interfaces are shown in Figure 1.

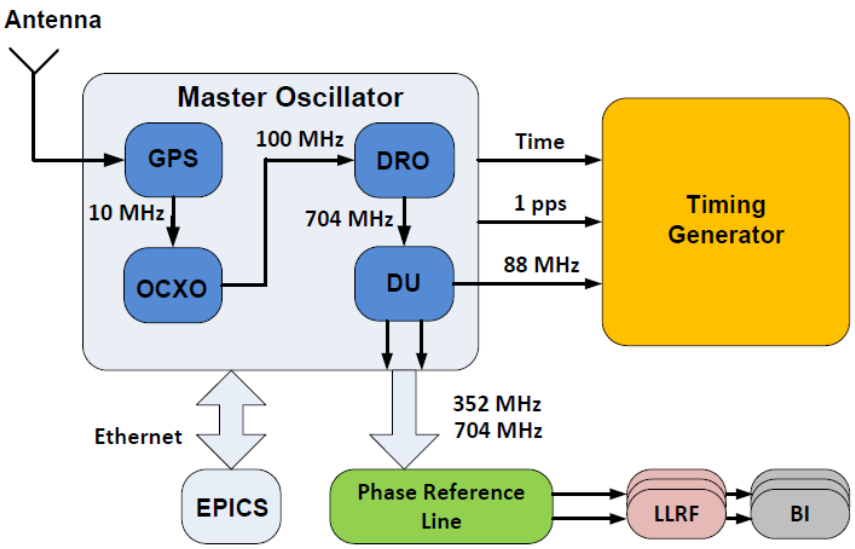


Figure 1 External interfaces of the MO

The master oscillator main building blocks and functions are:

- GPS with built-in Rb source provides accurate timing on a long time scale
- OXCO PLL with low jitter provides accurate timing on short time scale
- DRO PLL comprise low phase noise 704.42 MHz RF source
- Distribution Unit generates 352.21 MHz and 88.0525 MHz
- Ethernet interface to EPICS for monitoring and control

An overview of the external interfaces is given in Table 1.

Table 1 MO external interfaces

Interface	Type	Level	Details
GPS antenna input	50 Ω coaxial	See x.xx	TNC jack, L1:1575.42 MHz
GPS output	50 Ω, BNC female	+13 dBm ± 2 dB	10 MHz sinusoidal
AC supply	AC, 50 Hz	230VAC	AC with UPS
RF signals 704.42 MHz 352.21 MHz	 50 Ω, N female 50 Ω, N female	 +10 dBm +10 dBm	 sinusoidal sinusoidal
Timing Generator 1 PPS 88 MHz UTC	 50 Ω, BNC female 50 Ω, N female IPv4/IPv6, RJ-45	 Positive TTL pulse + 10 dBm TBD -	 20 us, 1 ms, 100 ms or 500 ms widths sinusoidal or square Time and date information
Ethernet	IPv4/IPv6, RJ-45	-	For monitoring and control

Critical design parameters for the Master oscillator are:

- Timing accuracy with jitter at femtosecond level
- Frequency accuracy and stability
- Availability
- Temperature drift, both amplitude and phase

The overall MO phase noise targets are given Appendix 7.1. To meet the high availability requirements of ESS redundancy will be used. Two Master Oscillators will be running in parallel and monitored, and only the unit having the best performance, judged by the monitoring system, will be in use. This is described in more detailed in section 6.

4. Hardware description

4.1 Electrical design

4.1.1 GPS disciplined Rb

There are several vendors providing COTS GPS units and for prototype testing the Meridian model from EndRun was chosen for cost and performance reasons.

The GPS needs also to provide complete time information to the EVG, including date and year, or else the time information needs to be set manually from EPICS. The Meridian model has several options to provide the time over Ethernet.

The EndRun Meridian GPS is disciplined by a Rubidium (Rb) source to obtain high timing stability and frequency accuracy in case the GPS signal is unavailable.

To improve close in phase noise performance the Meridian was purchased with a low phase noise option.

4.1.1.1 Antenna Interface

The antenna interface is coaxial 50 ohm and input connector type is TNC. The GPS uses L1 band at 1575.42 MHz. Cable lengths of up to 76 m (250 ft.) can be used without any external amplifiers if the provided integral +35 dB LNA antenna is used and cable types with less loss than 10dB/100ft. EndRun

recommends to use RG-59 cables from Belden, type 9104 for lengths up to 250 feet and 1505A for above (even though these are 75 ohm cables due to lower loss than RG-58 and long lengths makes reflections less critical). For details see EndRun user manual [1].

4.1.1.2 GPS output

The GPS output is 10 MHz sinusoidal with specified performance according to Table 2.

Table 2 GPS 10 MHz output performance

Parameter	Value	Comment
Stability w GPS signal	+/- $1*10^{-12}$	average 24h (Allan deviation)
Stability w/o GPS signal	+/- $2*10^{-11}$	average 24h (Allan deviation)
Phase noise, 1 Hz	-80 dBc/Hz	low phase noise option
10 Hz	-100 dBc/Hz	
100 Hz	-135 dBc/Hz	
1 kHz	-145 dBc/Hz	
10 kHz	-145 dBc/Hz	
100 kHz	-145 dBc/Hz	

4.1.2 OCXO PLL

4.1.2.1 OCXO PLL Overview

This unit consists of a voltage controlled OCXO, PLL, loop filter and resistive splitter as shown in Figure 2.

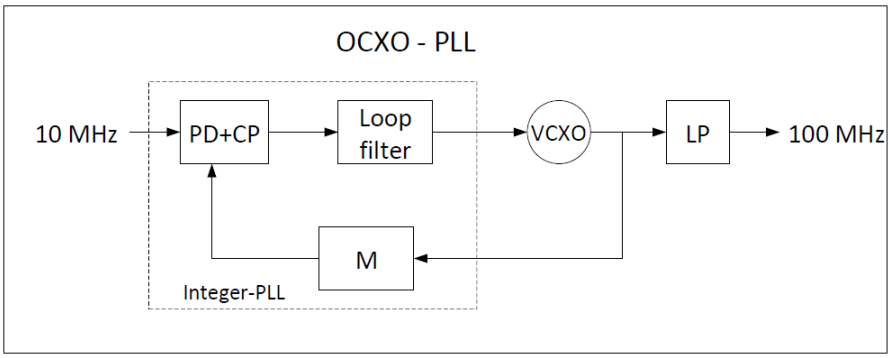


Figure 2 OCXO PLL overview

The OCXO is a SC-cut oven controlled VCXO with a nominal frequency of 100 MHz from NEL. It can be customized with different performances in respect to frequency stability over temperature, aging and phase noise. In Table 3 an overview of the chosen parameters are shown.

Table 3 OCXO main parameters

Parameter	Value	Comment
Stability over Temp	±10 ppb	+5 to +60 degC
Aging, per day	0.5 ppb/day	after 30 days
Aging, per year first year	100 ppb	
Aging, per year second year	30 ppb	

Phase noise, 1 Hz	-90 dBc/Hz	Standard version, option L
10 Hz	-120 dBc/Hz	
100 Hz	-135 dBc/Hz	
1 kHz	-142 dBc/Hz	
10 kHz	-150 dBc/Hz	

4.1.2.2 Pulling range budget

Stability budget for 15 years of aging including temperature drift:

Table 4 OCXO aging budget

Effect	**Frequency drift**	**Cumulative**
Stability temperature	±5 ppb	5 ppb
Aging, first year	100 ppb/year	100 ppb
Aging, year 2-6	30 ppb/year	150 ppb
Aging, year 7-15	15 ppb/year	135 ppb
Total		**390 ppb**

OCXO pull range is typical ±500 ppb and minimum ±300 ppb according to the data sheet. In practice it is not likely all the above contributors will drift in the same direction and at maximum rate every year, and even if they do, the PLL will be able to compensate for drifts over more than 15 years according to Table 4.

4.1.2.3 OCXO PLL Design

The OCXO PLL is implemented on the same PCB as the DRO and more details about the implementation can be found in the DRO section, 4.1.3.2.

The HMC1031 PLL from Hittite is used as it has a good performance and simple to use. The recommended input levels are given in Table 5 .

Table 5 PLL input levels

Input	**Level [dBm]**	**Details**
Reference	0	10 MHz, sinusoidal
VCO	-5	100 MHz, sinusoidal

The PLL has a +3.3V supply and to be able to utilize the full control voltage of 0.5 V to +4.5 V, instead of being limited to PLL CP range of 0.2 - 3.0 V with passive filter, an active loop filter is used. In Figure 3 an active filter with a DC control level is shown.

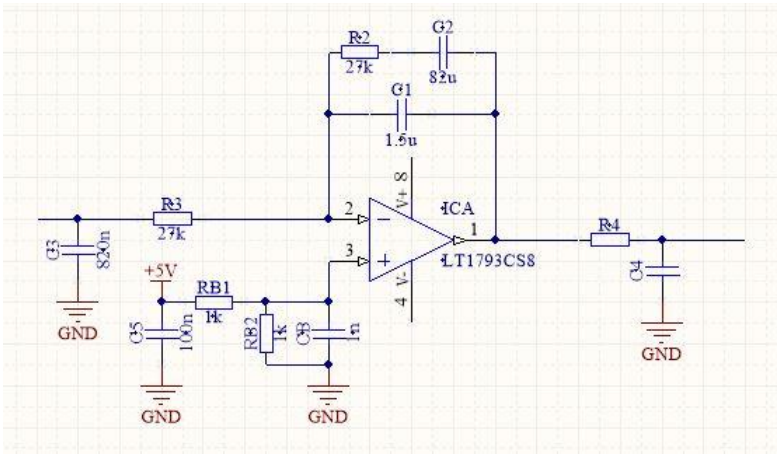


Figure 3 Loop filter with activeC topology

RB1=1k5 and RB2=1k gives 2.0V at the OP-amp input which is close to half the PLL supply voltage of 3.3V. Since the PLL is only supporting positive control slope an additional inverting OP-amp is needed as outlined in Figure 4.

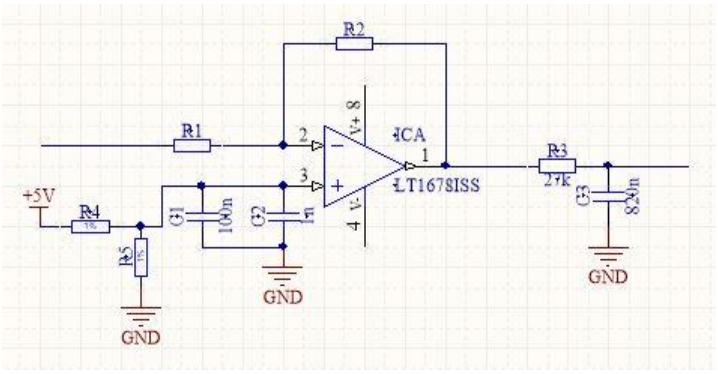


Figure 4 Inverter needed to get positive slope

A non-inverting filter topology is given in Figure 5 and has the advantage of not needing any additional inverter op-amp. It would also be possible to use passive loop filter but the drawback is limited voltage control of maximum +3.3V from the PLL circuitry and will limit the life time of the OCXO caused by aging. Both active filter topologies, with inverting and non-inverting OP-amps, will be evaluated for the final design.

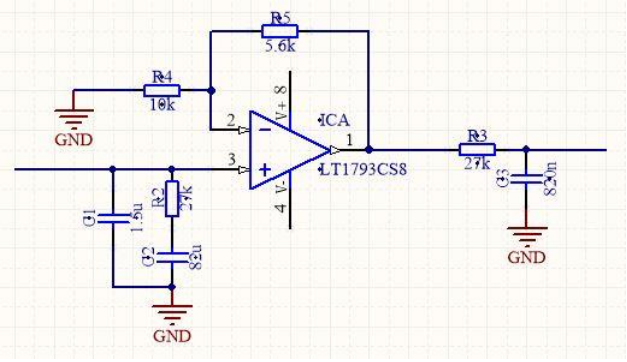


Figure 5 Loop filter with DC gain of 1.56

4.1.2.4 OCXO PLL Performance

The internal phase noise requirements of the OCXO are based on simulations. The black trace in Figure 6 shows the suggested requirements and phase noise numbers are also shown in Table 6.

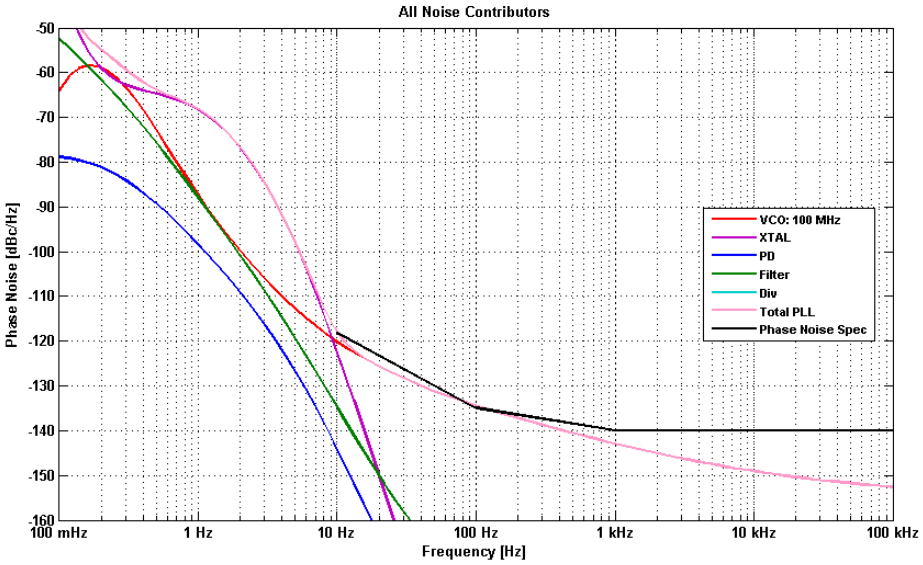


Figure 6 OCXO Phase noise with 0.4 Hz loop filer BW

Table 6 OCXO Phase noise requirement

Phase noise	Value	Comment
(1 Hz)	(-80 dBc/Hz)	Limited by Rb source
10 Hz	-118 dBc/Hz	
100 Hz	-135 dBc/Hz	
1 kHz	-140 dBc/Hz	
10 kHz	-140 dBc/Hz	
100 kHz	-140 dBc/Hz	

4.1.3 DRO PLL

4.1.3.1 DRO PLL Overview

A DRO topology is chosen for the high Q and thereby excellent phase noise performance. It is designed for 704 MHz since DR dimensions gets to large at lower frequencies.

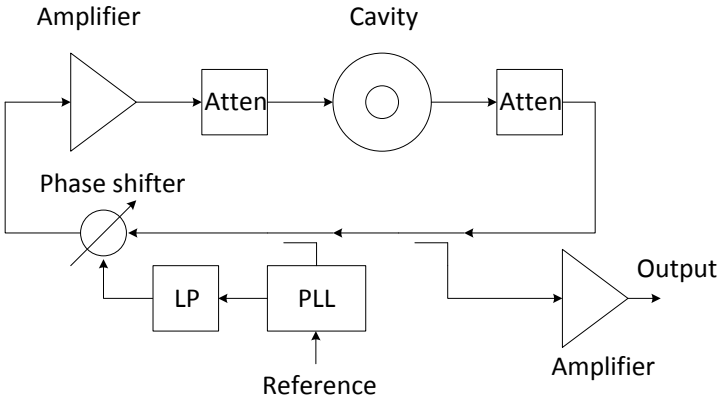


Figure 7 DRO block diagram

The tunable DRO contains following blocks:

- Resonator Cavity
- Amplifier
- Phase shifter
- Couplers
- PLL
- Loop filter (LP)
- Attenuators

4.1.3.2 DRO PLL interface

The external interface for DRO and OCXO is outlined in Table 7.

Table 7 DRO and OCXO interface

Interface	Input/Output	Level	Details
DC supply	Input	 +14 V +6 V	 < 300 mA < 1 A
10 MHz	Input	+ 10 dBm, sine-wave	From GPS
704.42 MHz	Output	+ 10 dBm, sine-wave	Sinusoidal
Monitoring DRO lock detect OCXO lock detect Temperature Supply voltages	Output	Digital or analog	Interface to DU

4.1.3.3 DRO PLL design

The DRO will be contained in a temperature regulated owenized compartment at +30 °C to minimize the thermal drift that could affect frequency, amplitude and phase stability. The plan is to use a COTS incubator for this. Even though the rack temperature will be regulated within +25 ± 1 °C it is believed an inner temperature control with regulation accuracy of ±0.5 °C will improve performance and especially if the rack temperature is suddenly changed, if for example the rack door is being opened.

Mechanical vibration could cause frequency or phase modulation and needs careful design of the mechanics. Some kind of rubber stands are considered to damp vibrations from the surroundings.

Other things to cover:
-Temperature behavior and aging set requirement of tuning range (aging covered by mechanical tuning?)

Open loop gain and phase delays:

Table 8 Gain and phase delay

Unit	Gain [dB]	Phase [degrees]
Amplifier, PSA	14.4	-52.0
Amplifier, BFG35	13.0	-67.8
Amplifier, BFP196	18.6	-79.6
Cavity1	-5.3	133.6
Cavity2	-6.3?	-
Phase shifter, 2.5V	-1.1	121.8
Phase shifter, 3.0V	-0.8	162.2
Attenuators	-3	~-22
Coupler1	-0.51	-102.5
Coupler2	-0.57	-119.9
Cable1	-	-
Cable2	-	-
PWB traces	-0.0	-0.0
Total excl. Cavity and Ampl.		

4.1.3.3.1 Resonator Cavity

A cylinder made of aluminum is used as resonator with a DR placed in the center. A picture of cavity and DR are shown in Table 7 below. The amounts of coupling from the microstrips to the DR are affecting the Q-factor of the DRO. Weaker coupling will reduce loading of the DR and increase loaded Q-factor. On the other hand increased insertion loss will increase the needed gain to start the oscillation. The support between DR and Cavity bottom is used to lift the DR from the ground plane. The distance between the microstrip and DR determines the coupling factor.

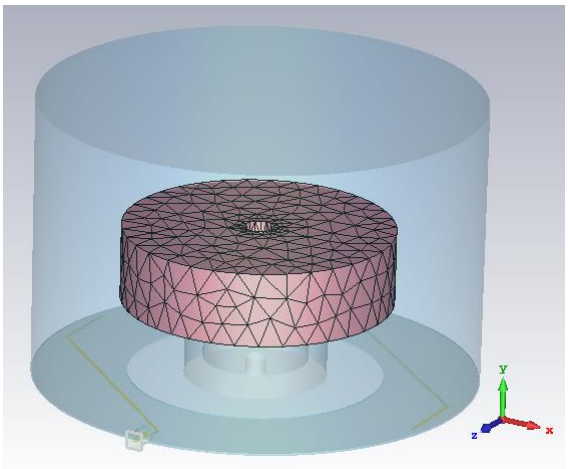


Figure 8 DRO block diagram

The mechanical dimensions of the DR and support are given in Table 9 and the electrical properties in Table 10.

Table 9 Dielectric resonator mechanical dimensions

DR dimensions	Inch
Outer diameter	3.358 +/- 0.025
Inner diameter	0.372 +/- 0.015
Thickness	0.951
Support, OD	
Support, ID	
Support, thickness	

Table 10 Dielectric resonator electrical parameters

DR properties	Sample	Lower spec	Upper spec
Dielectric constant E'	42.25	42.25	43.75
Tf lin (25◦C-60◦C)	0.37	-2.00	2.00
Q (in cavity)	26549	27000	N/A
Support, E'	N/A	9.x	9.x

-Mechanical tuning TBD

4.1.3.3.2 Amplifier

To achieve low close in phase noise the flicker noise of the amplifier must be kept low. A Si HBT transistor with moderate Ft is chosen for this reason. The collector current is also influencing Ft and the biasing point becomes a trade-off between linearity and phase noise. Three transistor candidates will be evaluated:

Transistor:	**Gain**
BFG35	13.0 dB
BFP196W	18.6 dB
PSA-509	14.4 dB

4.1.3.3.3 Phase shifter

The phase shifter has a LP filter topology to attenuate higher order modes in the resonator not causing additional oscillation.

The varactor diodes are biased from the PLL causing the capacitor between anode and cathode to change. This will introduce a variable phase shift and thus changing frequency of oscillation.

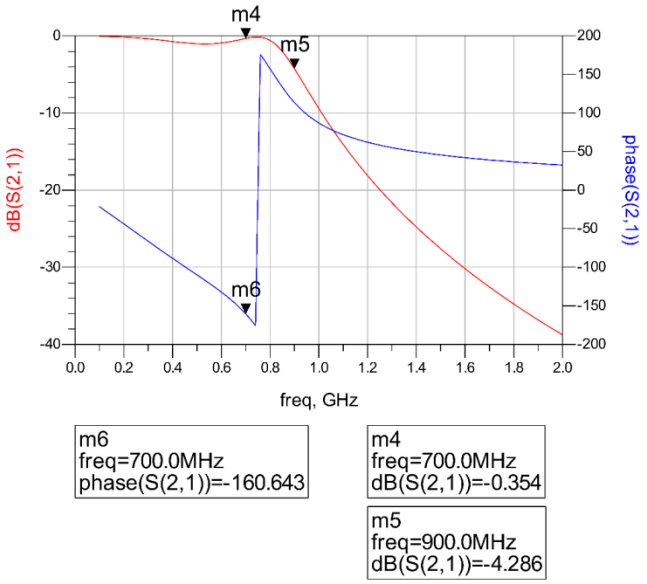


Figure 9 Phase shift simulation

The fixed component values in the simulation are L=15 nH and C=6 pF.

4.1.3.3.4 Couplers

Couplers are used for the output and PLL feedback signals to keep loop attenuation low, compared to splitters. Coupling factor of 10 dB gives a good trade-off between attenuation and margin to thermal noise level.

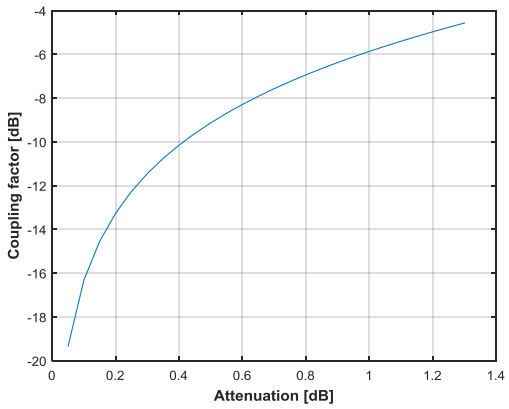


Figure 10 Coupler attenuation vs coupling factor

4.1.3.3.5 PLL

The PLL is a fractional-N HMC704LP4E with a reference signal from the OCXO. For a square input the recommended voltage swing is between 0.6 and 2.5 Vpp with a slew rate higher than 0.5V/ns. Typical RF input level is -7 dBm with a specified interval of -3 dBm to -15 dBm.

The PLL needs to be programmed when DC supply is provided and that will be done automatically by a micro controller on the same PCB.

4.1.3.3.6 Loop filter

A passive loop filter is used for simplicity and good noise properties. Analysis of the PLL and loop filter is shown in Appendix 7.2.

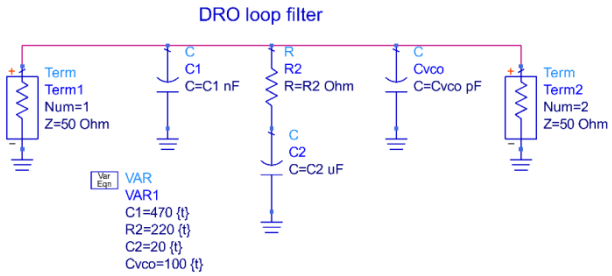


Figure 11 DRO loop filter

Table 11 DRO PLL loop filter values

C1	R2	C2
360 nF	220 Ω	20 uF

4.1.3.3.7 Attenuator

Since the cavity is under coupled and not perfectly matched to 50 ohm attenuators are used at the input and output of the cavity ports. The attenuators are also used to adjust the amount of excess gain of the amplifier. Resistor values are given in the table below for T and Pi networks with 5 % resistor tolerances.

Table 12 Attenuator values

Attenuation (dB)	T network		Pi network	
	Rs	Rp	Rs	Rp
1.0	2.9	420	5.6	910
1.5	4.2	290	9.1	560
2.0	5.6	220	12	420
2.5	6.8	180	15	350
3.0	8.2	150	18	300
5.0	15	82	30	180
7.0	20	56	43	130

4.1.4 Divider Unit

4.1.4.1 Divider Unit Overview

The Divider Unit generates 352 MHz and 88 MHz signals from the 704 MHz signal coming from the DRO. A block diagram of the Divider Unit is given below. DC inputs and Ethernet connection is not shown.

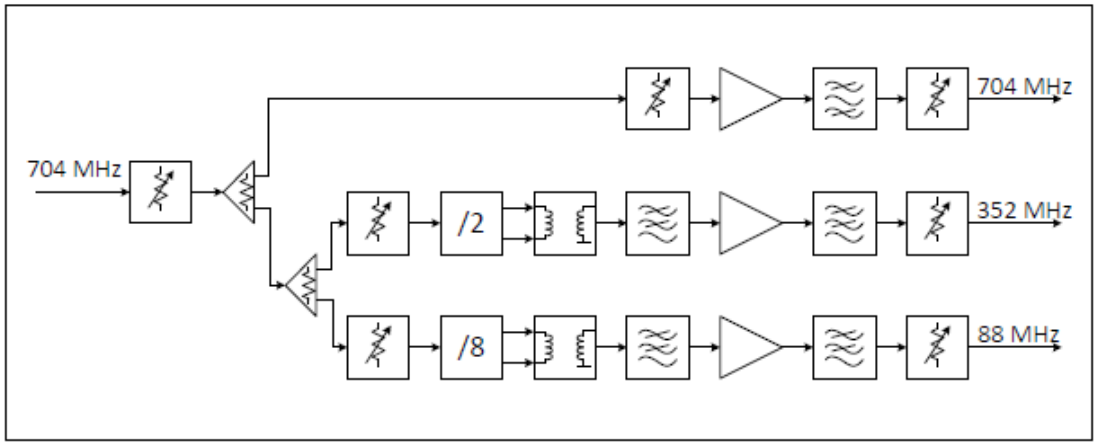


Figure 12 Divider Unit block diagram

4.1.4.2 Divider Unit interface

The external interface for Divider Unit is outlined in Table 7.

Table 13 DRO and OCXO interface

Interface	Input/Output	Level	Comments
DC supply	Input	+12 V	< TBD mA
704.42 MHz	Input	+ 10 dBm, sinusoidal	From DRO
88.0525 MHz	Output	+ 10 dBm, square **TBD**	To switch box
352.21 MHz	Output	+ 10 dBm, sinusoidal	To switch box
704.42 MHz	Output	+ 10 dBm, sinusoidal	To switch box
Monitoring 88 MHz level 352 MHz level 704 MHz level Temperature Supply voltages	Output	Ethernet	To EPICS

4.1.4.3 Divider Unit Design

Main components of the DU is:

- Power Splitters
- Divider AD9515 with LVPECL balanced output
- LP Filters to suppress harmonics
- Amplifiers with good linearity
- Monitoring of signal powers and voltage supplies (not shown in Figure 12)

The XT-Pico module will be used for monitoring over EPICS and have successfully been integrated at ESS by Beam Instrumentation and most of this work could be utilized.

4.1.5 Power Supply

All AC power should be provided from an UPS not to be effected by power outages.

External COTS power supplies units provide DC power to DRO and Distribution Unit.

4.1.6 Ethernet

The Ethernet connectivity used for control and monitoring will be provided by an XT-Pico board which have built in I2C interface. Following signals will be monitored:

- 704 MHz input signal power
- 704 MHz output signal power
- 352 MHz output signal power
- 88 MHz output signal power
- Critical voltage supplies
- Temperature

4.2 Mechanical design

4.2.1 Mechanical design of DRO and OCXO

DRO and OCXO is implemented on the same PCB, and placed directly underneath the DRO cavity in a metal housing with shared mechanical bottom. Connections between Cavity and DRO are made through holes in the bottom. All external connectors are placed on one side of the housing to ease the assembling of PCB connectors and mechanics.

4.2.2 Mechanical design of Distribution Unit

Traditional aluminum housing with N connectors for the RF signals.

5. Software description

5.1 EPICS

The plan is to integrate the XT-Pico board, which is already successfully used by Beam Instruments, to have full accessibility to control and monitoring over EPICS. By reusing the integration work only limited SW resources would be needed.

5.2 PLL programming

The DRO PLL will be programmed with a micro controller from Atmel automatically when the unit is powered up. During normal operation the micro controller will only be used for monitoring of internal signals.

The OCXO PLL does not need any programming.

6. Availability

Single module availability numbers and fault impact are shown in Table 14 below. In order to improve availability redundancy is suggested.

Table 14 MTBF of modules

Module	MTBF (hours)	Impact
GPS	>220 000	Minor time drift
OCXO	TBD	Machine stop
DRO	TBD	Machine stop
Distribution Unit	TBD	Machine stop

In order to improve availability there will be two MO's running at the same time. One being active, and the other as a hot spare. Both MO's will continuously be monitored and compared, and the unit having best performance will be used from a switch box as illustrated in Figure 13. The switch between units is done manually not to introduce extra complexity and failure probability.

Since the RF signals of the MO system is being amplified before entering the Phase Reference Line (PRL), and the amplifiers will have a big impact of the total availability, there could be reasons to also have redundancy for amplifier and make the switch after amplification. The amplifiers are belonging to the PRL system and these considerations needs to be done together with the PRL system, and are not in the scope for this document.

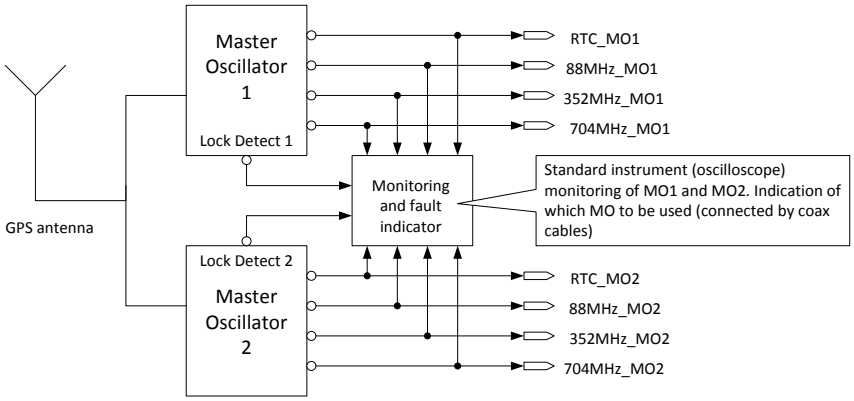


Figure 13 MO redundancy and monitoring

7. Appendixes

7.1 MO phase noise targets

Table 15 MO phase noise targets

Offset [Hz]	Phase noise [dBc/Hz]		
	88 MHz	352 MHz	704 MHz
10	-110	-98	-92
100	-123	-111	-105
1k	-148	-137	-135
10k	-156	-150	-155
100k	-162	-156	-160
1M	-162	-158	-165

7.2 DRO loop filter and phase noise simulations

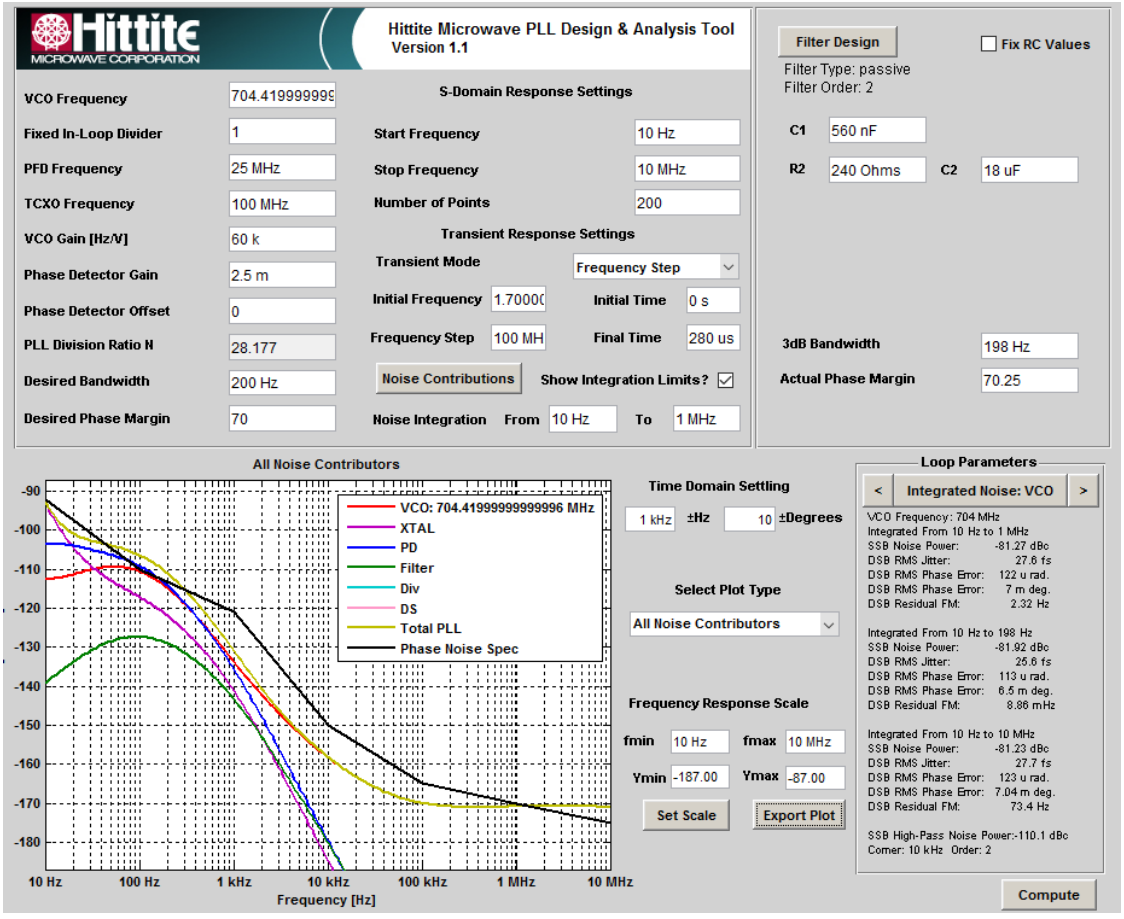
PhaseShifter: 100 degrees/V (voltage interval 3-4V ??)
Cavity: 588 Hz/degree (first version with S21: -5.3dB)

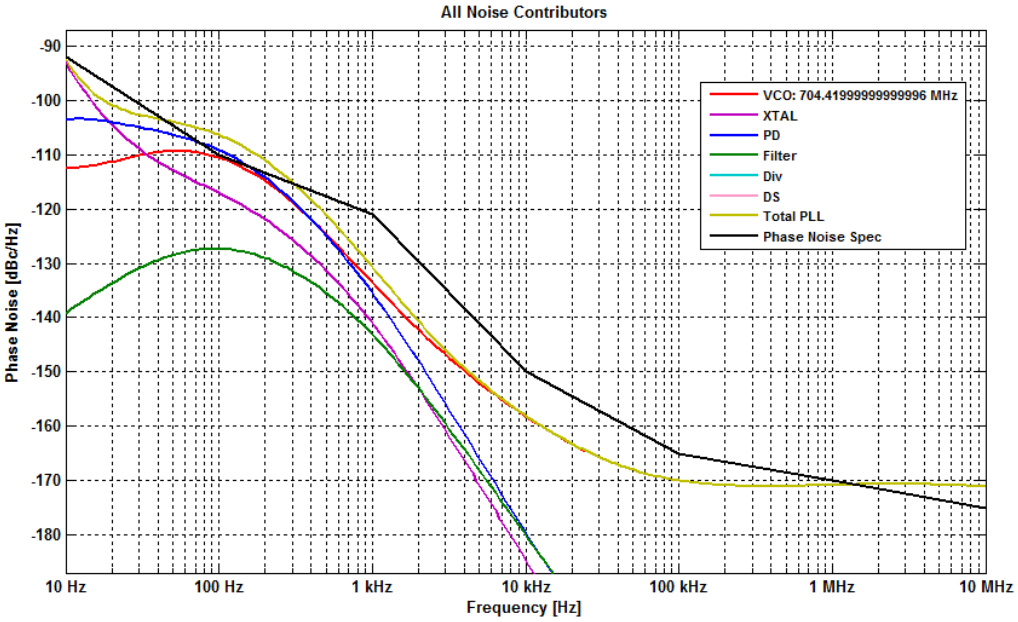
- ⇨ VCO gain: ~60 kHz/V

Cavity2: 650 Hz/degree (30 degrees over 20kHz, S21: -6.8dB)

- ⇨ VCO gain: ~65 kHz/V

Loop BW	100 Hz	200 Hz	700 Hz
C1	2.7 uF	560 nF	47 nF
R2	110 ohm	240 ohm	820 ohm
C2	82 uF	18 uF	1.5 uF




All Noise Contributors
Phase Noise [dBc/Hz]
-90
-100
-110
-120
-130
-140
-150
-160
-170
-180
10 Hz
100 Hz
1 kHz
10 kHz
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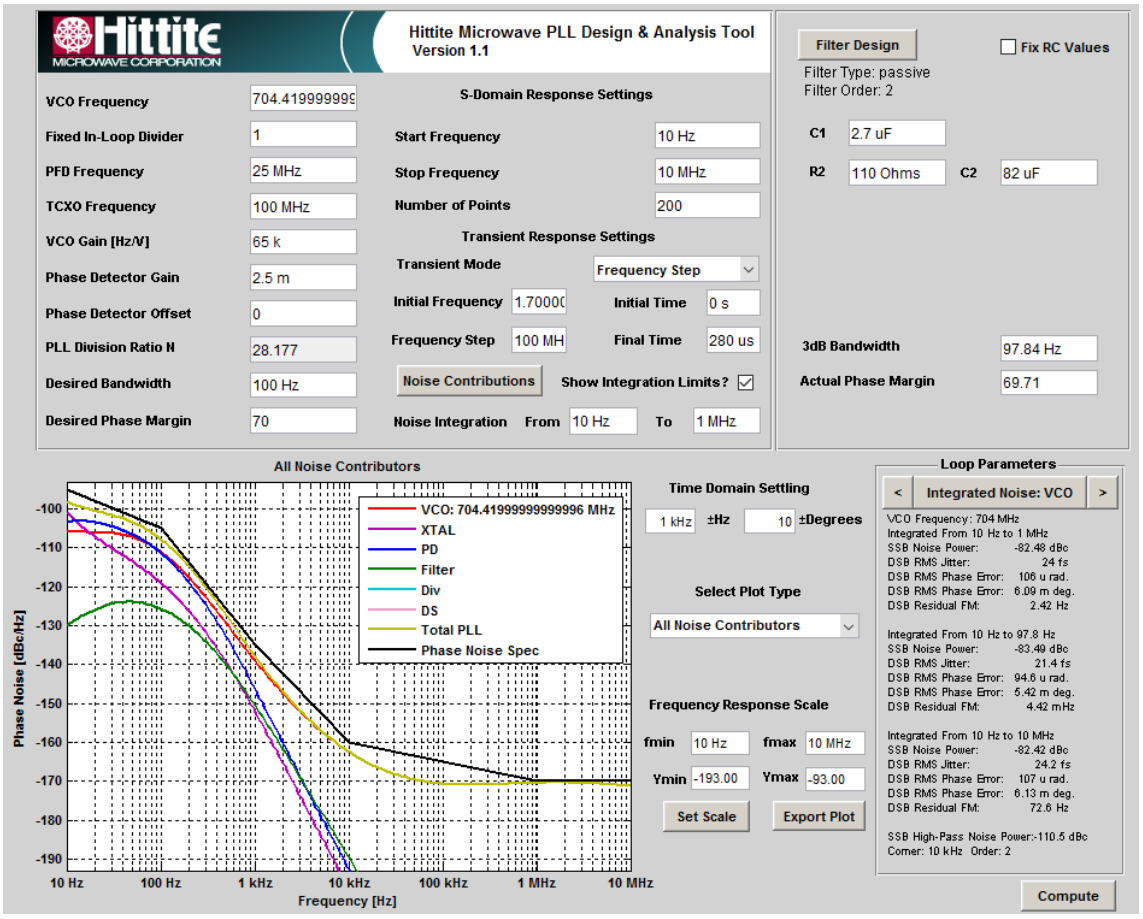
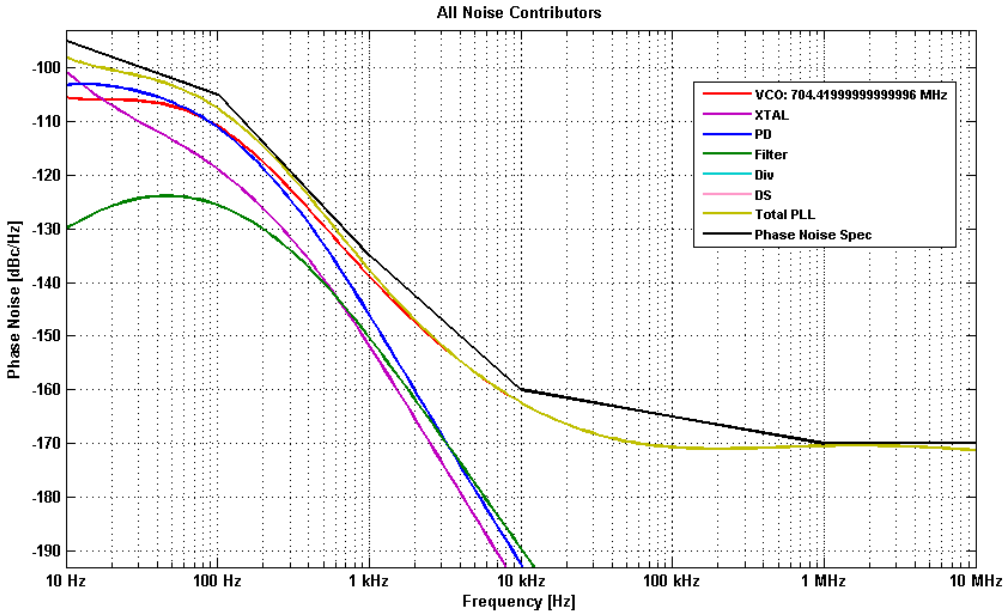
10 MHz
Frequency [Hz]
VCO: 704.41999999999996 MHz
XTAL
PD
Filter
Div
DS
Total PLL
Phase Noise Spec


Hittite MICROWAVE CORPORATION
Hittite Microwave PLL Design & Analysis Tool
Version 1.1
VCO Frequency
704.419999999
Fixed In-Loop Divider
1
PFD Frequency
25 MHz
TCXO Frequency
100 MHz
VCO Gain [Hz/V]
65 k
Phase Detector Gain
2.5 m
Phase Detector Offset
0
PLL Division Ratio N
28.177
Desired Bandwidth
100 Hz
Desired Phase Margin
70
S-Domain Response Settings
Start Frequency
10 Hz
Stop Frequency
10 MHz
Number of Points
200
Transient Response Settings
Transient Mode
Frequency Step
Initial Frequency
1.70000
Initial Time
0 s
Frequency Step
100 MH
Final Time
280 us
Noise Contributions
Show Integration Limits?
Noise Integration
From
10 Hz
To
1 MHz
Filter Design
Fix RC Values
Filter Type: passive
Filter Order: 2
C1
2.7 uF
R2
110 Ohms
C2
82 uF
3dB Bandwidth
97.84 Hz
Actual Phase Margin
69.71
All Noise Contributors
Phase Noise [dBc/Hz]
-100
-110
-120
-130
-140
-150
-160
-170
-180
-190
10 Hz
100 Hz
1 kHz
10 kHz
100 kHz
1 MHz
10 MHz
Frequency [Hz]
VCO: 704.41999999999996 MHz
XTAL
PD
Filter
Div
DS
Total PLL
Phase Noise Spec
Time Domain Settling
1 kHz
±Hz
10
±Degrees
Select Plot Type
All Noise Contributors
Frequency Response Scale
fmin
10 Hz
fmax
10 MHz
Ymin
-193.00
Ymax
-93.00
Set Scale
Export Plot
Loop Parameters
<
Integrated Noise: VCO
>
VCO Frequency: 704 MHz
Integrated From 10 Hz to 1 MHz
SSB Noise Power: -82.48 dBc
DSB RMS Jitter: 24 fs
DSB RMS Phase Error: 106 u rad.
DSB RMS Phase Error: 6.09 m deg.
DSB Residual FM: 2.42 Hz
Integrated From 10 Hz to 97.8 Hz
SSB Noise Power: -83.49 dBc
DSB RMS Jitter: 21.4 fs
DSB RMS Phase Error: 94.6 u rad.
DSB RMS Phase Error: 5.42 m deg.
DSB Residual FM: 4.42 mHz
Integrated From 10 Hz to 10 MHz
SSB Noise Power: -82.42 dBc
DSB RMS Jitter: 24.2 fs
DSB RMS Phase Error: 107 u rad.
DSB RMS Phase Error: 6.13 m deg.
DSB Residual FM: 72.6 Hz
SSB High-Pass Noise Power:-110.5 dBc
Corner: 10 kHz Order: 2
Compute



7.3 DRO unit design: schematic and PCB

Table 16 OCXO supply voltages

OCXO-PLL	Voltage (V)	Current (mA)	Power (mW)	Supply name	Comment
OCXO	+5	700 **TBC**	3500 **TBC**	P5Vocxo	Oven heating, only at startup
PLL, HMC1031	+3.3	2	7	P3V3pll	Ref in: 0 dBm; VCO in: -5 dBm
Op-amp LT1793	+5	5		P5Vloop	
OP-amp LT1678	+5	4		P5Vloop	
Led	+5	2	7	P5Vloop	

Table 17 DRO supply voltages

DRO-PLL	Voltage (V)	Current (mA)	Power (mW)	Supply name	Comment
Phase shifter	-	1	5		
PLL, HMC704	+3.3A +3.3D +5	58 7	200 35	P3V3A P3V3D P5VCP	Ref in: +6 dBm; VCO in: -7dBm 58 mA all +3.3V
Amplifier, loop	+12	100	1200	P12VA	Worst case current (PSA509)
Amplifier, output	+5	100	500	P5RF	ADL5611
u-processor	+3.3	<5	15	P3V3D	+1.8 to +5.5 supply
I2C driver	+5	<10	50	P5VD	I2C; 30mA sink current

Table 18 PCB power nets

Power net	Voltage (V)	Total current (mA)	Comment
PVhigh	+14 **TBA**		Input DC
PVlow	+6 **TBA**		Input DC
P12V	+12	120	output amplifier: 100 mA
P5Vvco -P5Vocxo -P5Vloop	+5	<720 ~100 11	Oven heating, warm up: 700mA
P5V -P5VRF -P5VCP -P5VD	+5	<120 100 7 10	(max: PSA509)
P3V3 - P3V3A - P3V3D -P3V3pll	+3.3	<80 58 <20 **TBD** 2	PLL digital and u-controller

Power Net	LDO	Voltage (V)	Current (mA)	LDO current (mA)	Power dissipation
P12V	ADP7118	+12	120	<200	0.24 W; **Vin=14V**
P5Vvco	ADM7150	+5	720 (100)	<800	0.1 W, 0.72 W peak; **Vin=6V**
P5V	ADP7118	+5	120	<200	0.12 W; **Vin=6V**
P3V3	ADP7118	+3.3	80	<200	0.22 W; **Vin=6V**

PCB Layout Layers:

Table 19 PCB layout layers

Name	Layer (Altium)	Comment
Top layer	Top Layer	Footprint etc
Solder paste	Top Paste	Same as footprint
Solder mask opening	Top Solder	“negative”
Component designator (silkscreen)	Top Overlay	Silkscreen
Keep out	Mechanical 15	and component origin
Component orientation	Mechanical 14	Polarity
Component body	Mechanical 13	3D view
RF ground	TBD layer	
Inner signal planes	TBD layer	
Power planes	TBD layer	
Bottom layer	Bottom layer