PDR for Cavity Simulator

Maciej Grzegrzółka
Lund, 30.05.2017
Agenda

- Introduction
- Hardware
- Firmware and Software
- Design Status
• PEG will assemble and install 80 LLRF control systems.
• Each system will be tested after the assembly and then after the installation.
• To simulate the closed loop operation the Cavity Simulator is needed.
Introduction – Simulated System
Introduction – Block Diagram

Analog Front-end

Analog Input Signals

ADC
ADC
ADC
ADC

Analog Front-end

DSP UNIT

Cavity and Amplifier Model

DAC
DAC
DAC
DAC

Controller

Ethernet

PC

Analog Front-end

Analog Output Signals
Introduction – Requirements

- **RF outputs:**
  - Number of outputs: 6 (main) + 6 (monitoring)
  - Maximum output power: 15 dBm (main), 5 dBm (monitoring)
  - Center frequency: 704 MHz
  - Bandwidth: 10 MHz

- **RF inputs:** 2
  - Number of inputs: 2
  - Center frequency: 704 MHz
  - Bandwidth: 10 MHz

- **High Voltage analog inputs**
  - Number of inputs: 2
  - Voltage range: ±100 V
  - Bandwidth: 100 kHz
Introduction – Requirements

• Fast analog outputs:
  – Number: 2
  – Bandwidth: 1 MHz

• Analog outputs:
  – Number: 1
  – Bandwidth: 100 kHz

• Communication interfaces:
  – Ethernet
  – USB (JTAG)

• Power supply: 230 V

• Power consumption: <250 W
The latency of the real system is around 0.35 µs*.

It is equal to around 41 clock cycles at 117.4 MHz

Latency of typical ADC: 10 clock cycles

Latency of typical DAC: 7 clock cycles

Latency of the DSP: < 24 clock cycles

* Friedrik Kistensen, "LLRF performance evaluation"
## RF Signal Generation Schemes

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct Digital Synthesis</td>
<td>• Very simple analog circuit</td>
<td>• High sampling rate DAC required</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• High data rates</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Poor noise performance</td>
</tr>
<tr>
<td>Up-conversion</td>
<td>• Very good noise performance</td>
<td>• Complex analog circuit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Additional LO signal required.</td>
</tr>
<tr>
<td>Vector Modulator</td>
<td>• Simple analog circuit</td>
<td>• Two DACs required</td>
</tr>
<tr>
<td></td>
<td>• Good noise performance</td>
<td>• Reference signal required.</td>
</tr>
</tbody>
</table>

The Vector Modulator scheme was selected
## RF Signal Digitizing Schemes

<table>
<thead>
<tr>
<th></th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Direct Sampling</strong></td>
<td>• Very simple analog circuit</td>
<td>• Require high speed ADC</td>
</tr>
<tr>
<td><strong>Down Conversion</strong></td>
<td>• Very good noise performance</td>
<td>• Complex analog circuit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Requires additional LO signal generator</td>
</tr>
<tr>
<td><strong>IQ Demodulation</strong></td>
<td>• Simple analog circuit</td>
<td>• Require two ADCs</td>
</tr>
<tr>
<td></td>
<td>• Good noise performance</td>
<td>• Require Reference Signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Poor intermodulation performance</td>
</tr>
</tbody>
</table>

The down conversion scheme was selected.
Hardware – Block Diagram
# Hardware – FPGA Processing Module

<table>
<thead>
<tr>
<th></th>
<th>KC705</th>
<th>ZC706</th>
<th>ZCU102</th>
<th>KCU105</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>Kintex 7 XC7K325T</td>
<td>Zynq 7000 XC7Z045</td>
<td>Zynq Ultrascale XCZU9EG</td>
<td>Kintex Ultrascale XCKU040</td>
</tr>
<tr>
<td>CPU</td>
<td>-</td>
<td>Dual-core ARM Cortex-A9 MPCore</td>
<td>Quad-core ARM Cortex-A53</td>
<td>-</td>
</tr>
<tr>
<td>Logic Cells (K)</td>
<td>356</td>
<td>350</td>
<td>600</td>
<td>530</td>
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<tr>
<td>Block Ram (Mb)</td>
<td>25.74</td>
<td>19.1</td>
<td>32.1</td>
<td>21.1</td>
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<tr>
<td>DSP Slices</td>
<td>1440</td>
<td>900</td>
<td>2520</td>
<td>1920</td>
</tr>
<tr>
<td>RAM Type</td>
<td>DDR3</td>
<td>DDR3</td>
<td>DDR4</td>
<td>DDR4</td>
</tr>
<tr>
<td>RAM Capacity</td>
<td>1 GB</td>
<td>2 x 1 GB</td>
<td>4 GB+512 MB</td>
<td>2 GB</td>
</tr>
<tr>
<td>FMC Connectors</td>
<td><strong>HPC:</strong> 58 x LVDS, 4 x GT <strong>LPC:</strong> 34 x LVDS, 1 x GT</td>
<td><strong>HPC:</strong> 34 x LVDS, 8 x GT <strong>LPC:</strong> 34 x LVDS, 1 x GT</td>
<td><strong>HPC:</strong> 34 x LVDS, 8 x GT <strong>HPC:</strong> 34 x LVDS, 8 x GT <strong>LPC:</strong> 34 x LVDS, 1 x GT</td>
<td><strong>HPC:</strong> 57 x LVDS, 8 x GT <strong>LPC:</strong> 34 x LVDS, 1 x GT</td>
</tr>
</tbody>
</table>
Hardware – FPGA Processing Module

Source: https://wwws.samtec.com/standards/xilinx.aspx
Hardware – Data Converters Module

• 7 vector modulator channels,
• 4 fast ADCs,
• 2 fast DACs,
• 2 slow ADCs,
• 2 slow DACs,
• clock generation circuit,
• reference signal distribution circuit.
Hardware – Data Converters Module

7 x VM OUTPUT
7 x VM MONITORING OUTPUT
REFERENCE INPUT
2 x CLOCK INPUT
2 x CLOCK OUTPUT
4 x FAST ADC INPUT
2 x SLOW ADC INPUT
2 x FAST DAC OUTPUT
2 x SLOW DAC OUTPUT
8 x REMOTE I2C BUS OUTPUT

7 x VECTOR MODULATOR
CLOCK DISTRIBUTION
4 x FAST ADC
2 x SLOW ADC
2 x FAST DAC
2 x SLOW DAC
FPGA

2 x FMC CONNECTOR
Data Converters Module – Vector Modulator

![Diagram of Data Converters Module – Vector Modulator](image-url)
### Data Converters Module – Vector Modulator DAC

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Sampling Rate [MSPS]</th>
<th>NSD [dBc/Hz]</th>
<th>SFDR [dBc]</th>
<th>IMD</th>
<th>Latency [clock cycles]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAC3282</td>
<td>625 (x2 Interpolation)</td>
<td>-150</td>
<td>-64</td>
<td>-69</td>
<td>38</td>
</tr>
<tr>
<td>DAC3283</td>
<td>800 (x4 Interpolation)</td>
<td>-160</td>
<td>-72</td>
<td>-86</td>
<td>59</td>
</tr>
<tr>
<td>DAC5682Z</td>
<td>1000 (x2 Interpolation)</td>
<td>---</td>
<td>-77</td>
<td>-67</td>
<td>78</td>
</tr>
<tr>
<td>DAC3482</td>
<td>1250 (x2 Interpolation)</td>
<td>-155</td>
<td>-72</td>
<td>-77.5</td>
<td>140</td>
</tr>
<tr>
<td>AD9146</td>
<td>1200 (x4 Interpolation)</td>
<td>-164</td>
<td>-67</td>
<td>-81</td>
<td>64</td>
</tr>
<tr>
<td><strong>AD9783</strong></td>
<td>500</td>
<td>-165</td>
<td>-80</td>
<td>-86</td>
<td>7</td>
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<tr>
<td>AD9747</td>
<td>250</td>
<td>-165</td>
<td>-82</td>
<td>-86</td>
<td>7</td>
</tr>
</tbody>
</table>
## Data Converters Module – Vector Modulator Chip

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Bandwidth [MHz]</th>
<th>Noise Floor [dBm/Hz]</th>
<th>Uncalibrated Carrier Suppression [dBc]</th>
<th>Uncalibrated Sideband Suppression [dBc]</th>
<th>P1dB [dBm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRF370317</td>
<td>400 – 4000</td>
<td>-163</td>
<td>40</td>
<td>45</td>
<td>12</td>
</tr>
<tr>
<td>TRF370417</td>
<td>50 – 6000</td>
<td>-162</td>
<td>38</td>
<td>50</td>
<td>12</td>
</tr>
<tr>
<td>TRF370315</td>
<td>350 – 4000</td>
<td>-163</td>
<td>40</td>
<td>40</td>
<td>9</td>
</tr>
<tr>
<td>TRF370333</td>
<td>350 – 4000</td>
<td>-163</td>
<td>40</td>
<td>40</td>
<td>9</td>
</tr>
<tr>
<td>HMC1097</td>
<td>100 – 6000</td>
<td>-160</td>
<td>40</td>
<td>40</td>
<td>11</td>
</tr>
<tr>
<td>LTC5598</td>
<td>5 – 1600</td>
<td>-165</td>
<td>55</td>
<td>50</td>
<td>8.5</td>
</tr>
<tr>
<td>LTC5588-1</td>
<td>200 – 6000</td>
<td>-160</td>
<td>45</td>
<td>53</td>
<td>8.6</td>
</tr>
<tr>
<td>Part Number</td>
<td>Sampling Rate [MSPS]</td>
<td>SNR @ 70 MHz [dBFS]</td>
<td>SINAD @ 70 MHz [dBFS]</td>
<td>ENOB @ 70 MHz</td>
<td>SFDR @ 70 MHz [dBFS]</td>
</tr>
<tr>
<td>-------------</td>
<td>----------------------</td>
<td>---------------------</td>
<td>-----------------------</td>
<td>--------------</td>
<td>-----------------------</td>
</tr>
<tr>
<td>AD9652</td>
<td>310</td>
<td>75</td>
<td>74.6</td>
<td>12.1</td>
<td>87</td>
</tr>
<tr>
<td>ADS42LB69</td>
<td>250</td>
<td>75.5</td>
<td>74.2</td>
<td>12 (170 MHz)</td>
<td>90</td>
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<tr>
<td>ADC16DV160</td>
<td>160</td>
<td>76</td>
<td>75</td>
<td>-----</td>
<td>95</td>
</tr>
<tr>
<td>ADS42JB69</td>
<td>250</td>
<td>75.6</td>
<td>75.3</td>
<td>12 (170 MHz)</td>
<td>88</td>
</tr>
</tbody>
</table>
Data Converters Module – Clock Distribution

REF IN

CLK 1 IN

CLK 2 IN

VM1 CLK
VM2 CLK
VM3 CLK
VM4 CLK
VM5 CLK
VM6 CLK
VM7 CLK
CLK OUT1
FMC CLK1
FMC CLK2
FPGA CLK1
FAST DAC CLK

JADC CLK
ADC CLK
FMC CLK3
FMC CLK4
GTX CLK
CLK OUT2
SLOW ADC1 CLK
SLOW ADC2 CLK
SLOW ADC1 CNV
SLOW ADC2 CNV
FPGA CNV

LMK04808

PLL
Data Converters Module – Power Supply

- Voltage: 12 V
- Input current: 5.35 A
- Power dissipation: 64.2 W
The power dissipation of the module is around 64 W.

A cooling solution, utilizing BGA heatsink connected directly to GND plane was proposed.

The board to test the cooling solution has been designed and manufactured.
# Data Converters Module – Cooling

<table>
<thead>
<tr>
<th>Power dissipated</th>
<th>No heatsink, no forced airflow</th>
<th>No heatsink, forced airflow</th>
<th>Heatsink, no forced airflow</th>
<th>Heatsink, forced airflow</th>
</tr>
</thead>
<tbody>
<tr>
<td>0W</td>
<td>23,9 °C</td>
<td>23,9 °C</td>
<td>23,8 °C</td>
<td>23,8 °C</td>
</tr>
<tr>
<td>10W</td>
<td>85,2 °C</td>
<td>-</td>
<td>60,6 °C</td>
<td>-</td>
</tr>
<tr>
<td>25W</td>
<td>-</td>
<td>74,6 °C</td>
<td>-</td>
<td>50,8 °C</td>
</tr>
<tr>
<td>Thermal resistance</td>
<td>6,13 °C/W</td>
<td>2,03 °C/W</td>
<td>3,68 °C/W</td>
<td>1,08 °C/W</td>
</tr>
</tbody>
</table>

- The expected temperature rise for final board is:
  - Heat sink, no forced airflow: **40 °C**
  - Heat sink, forced airflow: **11.7 °C**
- For additional protection several temperature sensors are placed on board.
Hardware – Down Converter Module
Hardware – LO Generation Module
LO Generation Module - Clock Signal Phase Noise

![Graph showing phase noise vs frequency for two scenarios: Two stage divider using HMC794 and Converted reference.](image-url)
LO Generation Module - LO Signal Phase Noise

IF 32.02 MHz

Phase Noise (dBc/Hz)

Frequency (Hz)

Converted Reference
LO signal
Hardware – Reference Generation Module

![Diagram of Reference Generation Module]

- **EXT XO IN** connected to **XO**
- **LMX2592 PLL** connected to **EXT PLL**
- **EXT REF IN** connected to **4X REF OUT**
Reference Generation Module – Reference Signal Phase Noise

-20.00 dBc/Hz  Ref -20.00 dBc/Hz

1: 10 Hz -96.4724 dBc/Hz
2: 1 MHz -150.5547 dBc/Hz
X: Start 10 Hz
Stop 1 MHz
Center 500.005 kHz
Span 999.99 kHz

Noise Analysis Range X: Band Marker
Analysis Range Y: Band Marker

Avg Noise: -51.5492 dBc / 1 MHz
RMS Noise: 1.1568 mrad
RMS Jitter: 254.266 Fs
Residual FM: 53.6792 Hz
Hardware – External PLL

![Diagram of External PLL with DRO 2.816 GHz, REF IN, PLL OUT, and 4-port division]

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PDR for Cavity Simulator
External PLL – Phase Noise Measurements

Carrier 794.419954 MHz  1.2646 dBm

1: 10 Hz  -92.2729 dBc/Hz
2: 1 MHz  -161.3171 dBc/Hz
3: 10 Hz  -92.2729 dBc/Hz
4: 1 MHz  -161.3171 dBc/Hz
5: Center 500.005 kHz
6: Span 999.99 kHz

--- Noise ---
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -65.5524 dBc / 1 MHz
RMS Noise: 746.267 μrad
42.758 mdeg
RMS Jitter: 168.61 fssec
Residual FM: 7.4813 Hz

30.05.2017, Lund
PDR for Cavity Simulator
Hardware – Power Supply Module
• Two FPGAs are used in the Cavity Simulator:
  – Xilinx Kintex Ultrascale in the FPGA Processing Module,
  – Xilinx Artix 7 in the Data Converters Module.
• The FPGA Processing Module is responsible for:
  – communication with a PC,
  – gathering data from ADCs,
  – sending data to vector modulators,
  – data acquisition,
  – digital signal processing for cavity simulation.
• the Data Converters Module is responsible for:
  – communication with other modules,
  – forwarding data from slow ADCs,
  – forwarding data to DACs,
  – configuration of all modules.
Firmware – FPGA Processing Module

Legend:
- Blue: Analog Signals
- Green: IQ Signals
- Purple: DAC/ADC Signals
- Black: Digital Signals
- Red: Synchronization Signals

Diagram showing the flow of signals through the FPGA Processing Module, including connections for LLRF In, RF In, RF Reference In, Sync In, Sync Out, and outputs for LLRF Drive, Amplifier Modulator Out, Amplifier In, Amplifier Forward, Amplifier reflected, Cavity, Pezzo In, and DAQ.
Firmware – Data Converters Module

FPGA Processing Module

Legend:
- Analog Signals
- DAC/ADC Signals
- Digital Signals
Two software tools are provided to control the cavity simulator:

- **Standalone application**
  - Easy control over the device using graphical user interface.

- **API for integration with other systems**
  - Dedicated tool for integration with complex systems, for example the LLRF systems test stand.
  - The detailed description of this tool will be ready when the final scope of test is agreed.
Design Status

- 4 modules are being currently under development:
  - Data Converters Module:
    - Schematics: ready
    - PCB: design in progress
  - LO Generation Module:
    - Schematics: ready
    - PCB: ready for manufacturing.
  - Reference Generation Module.
    - Schematics: ready
    - PCB: design in progress
  - Power Supply Module.
    - Main components selected
    - Performance verification in progress
Design Status – Data Converters Module
Design Status – LO Generation Module
Conclusions

• Concept of the Cavity Simulator was presented
• Measurement results of the expected phase noise of the reference, LO and clock signals were shown.
• The hardware modules design is in progress.
• The firmware development will start after the Data Converters Module design is ready.
Thank You