

EUROPEAN SPALLATION SOURCE

Control/Timing Demonstrator

IKON13 27th September 2017 Steven Alcock (DG)

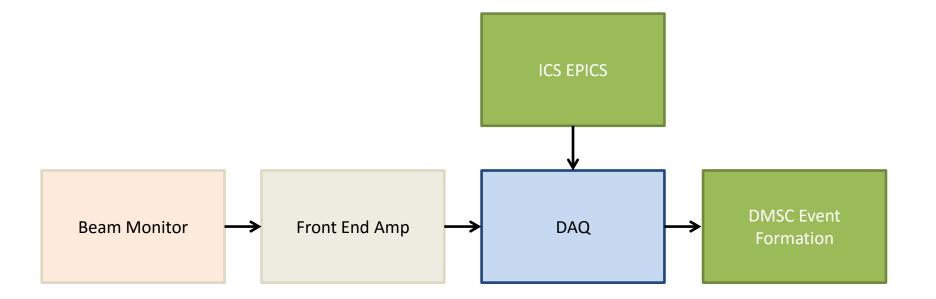
Motivation



- ESSIIP is an ICS project for developing and evaluating integration for relevant stakeholders (Detector Group, Choppers, Motion Control, Sample Environment, and the DMSC) – David Brodrick is coordinating this.
- Detector Group Readout produced a system to prove ICS interfaces (synchronous time distribution and control).
- The resulting system provides ADC readout for a small number of channels and hence could be used for evaluating beam monitors or other detectors.

ESSIIP ADC Readout Demonstrator Architecture

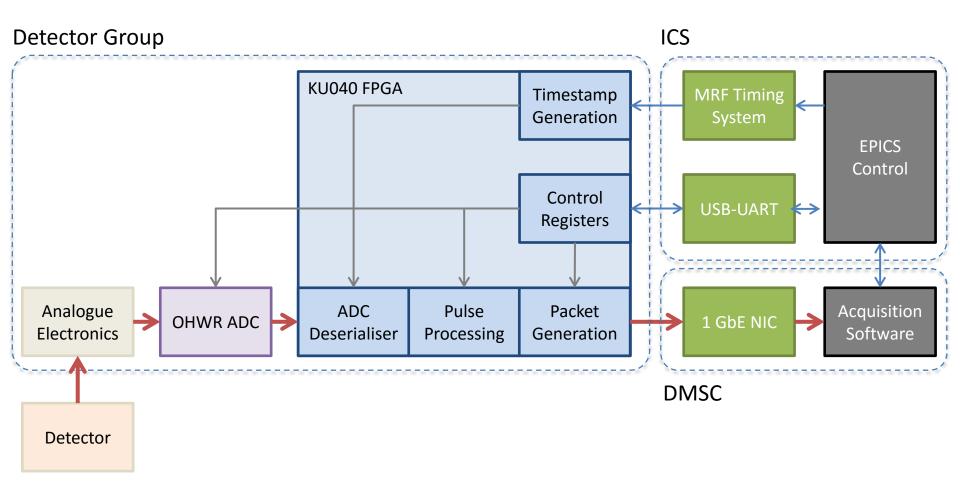




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ESSIIP ADC Readout Demonstrator Architecture





Key Features

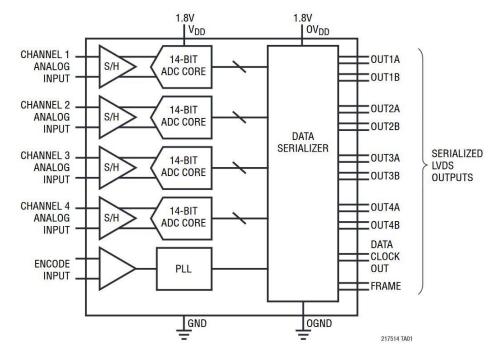


• ADC

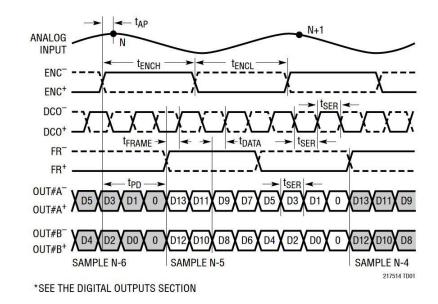
- Open Hardware (CERN) design
- Four channels, 30 MHz analog bandwidth
- 14-bit resolution
- 105 MHz sample rate we use 44 MHz from ICS timing system
- Programmable gain and offset
- FMC connector to FPGA.
- FPGA
 - Avnet KU040 development board
 - Configurable pulse detection/zero suppression to reduce data rate
 - Maximum pulse length of 65,536 samples (1.49 ms)
 - Channels read out pairwise depending on pulse activity
 - Synchronous clocking and timestamping from ICS reference signals
 - Custom readout protocol sent via standard Ethernet/IP/UDP.

Linear Technology LTC217X-14 ADC





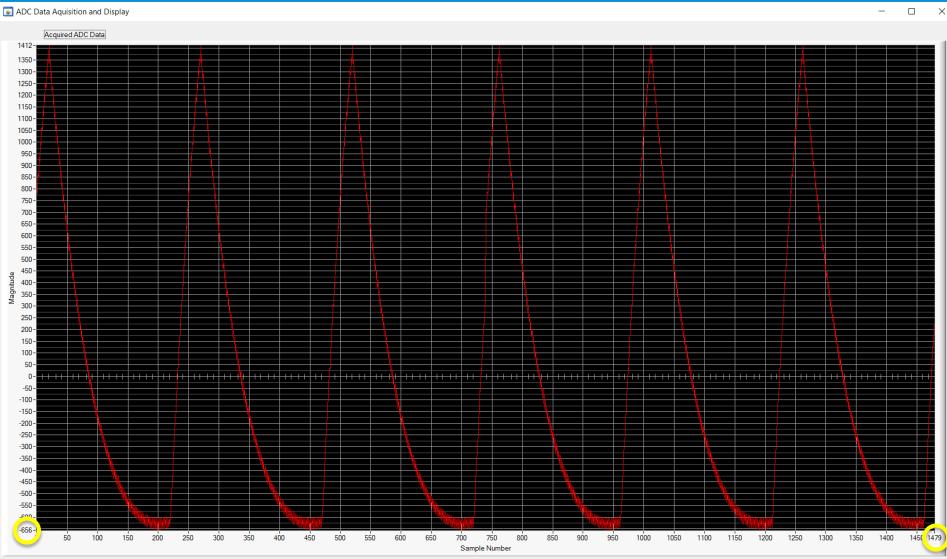
2-Lane Output Mode, 16-Bit Serialization*



Steven Alcock, Detector Group, 6th September 2017, source: http://cds.linear.com/docs/en/datasheet/21754314fa.pdf

Zero Suppression (1/2)





Number of dropped packets: 0000

Reset FPGA ADC BK4064 Config

Readout Config O Save Raw PCAP Set Raw PCAP Save Path

Set Raw PCAP Save Path Number of Packets to Acqui 3 2

Acquire QUIT

Zero Suppression (2/2)

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Acquired ADC Data 1405-1350-1300-1250--1200t 1150-1100-1050 1000 950-900ł 850-800-750 700 650 1 600 itude T 550 Magr I + 1 500 450-400-350ł 300-250· -200--1 150-100-50 1 <mark>╶╶╴╶╷╴╎╴╴╶╶╎╵╴╴╶╷╝</mark>╻╴╸╶╶╎╸<mark>╝</mark>╸╴ <mark>╞┼╴┼┼╎┼╴┼┼╎┽╴┼┼╎┽╴┽┼<mark>╬</mark>╴┼┼╎┽╴<mark>╔</mark>╎┼┽╶┼╎┼╸┼┼╎┽╴┼┤</mark> ++++1 <u>╶╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴╴</u> 0--50--100--150-_ -200-. -250 -300--333-7 0 791 60 120 160 180 200 220 240 260 320 360 420 440 460 480 500 520 560 580 600 620 640 660 680 700 720 740 20 40 80 100 140 280 300 340 380 400 540 760 Sample Number

Readout Config

Number of dropped packets: 0000

ADC Data Aquisition and Display

Reset FPGA ADC BK4064 Config

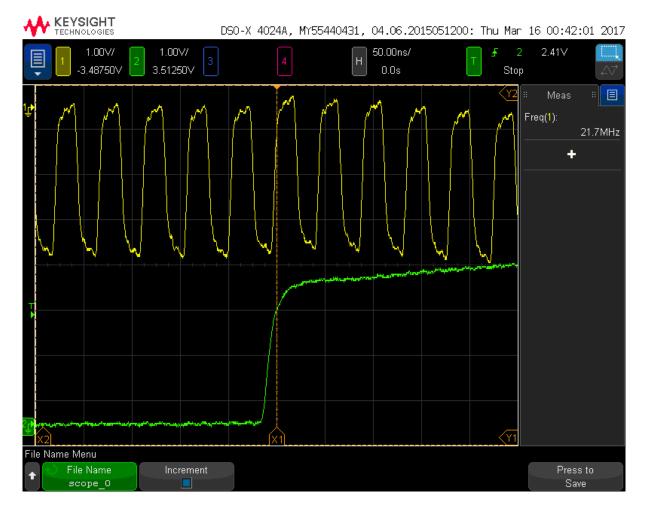
O Save Raw PCAP Set Raw PCAP Save Path Number of Packets to Acqui

Acquire

6

Timestamp Signalling





Data Packing



Ethernet IP	UDP	Readout	Data	Data
Header Header	Header	Header	Header	Payload

• Same as 100 G Demonstrator, but with meaningful data headers and payloads.

Туре	Word Count	
Sequence	Index	
Header Magic Word (0xABCD)	Pulse Width (in samples)	
Channel Number (0, 1, 2, 3)	Fragment Count	
Fractional Timestamp High	Fractional Timestamp Low	
Sample 0	Sample 1	
	Sample n-1	
Trailer High (OxBEEF)	Trailer Low (0xCAFE)	

To Do List



- Automatic ADC calibration
- Timestamp accuracy verification
- ADC resolution verification
- Software processing and data visualisation
- Readout of all four channels (implemented but not tested)
- Integration and test with a real detector.

Conclusion



- The system can provide synchronous readout for a small number of ADC channels.
- The control and timing interfaces from the ICS EPICS environment have been proven.