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## STATUS REPORT on the

## WIRE SCANNER ACQUISITION SYSTEM

## part of the ELETTRA to ESS IKC

# Mario Ferianis

on behalf of the Elettra ESS WS Team,

R. De Monte, S. Grulja and S. Cleva





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### THE BIG TEAM: URGENT UPDATE NEEDED !!!

	WBS 11.7.7	Rev. 1.2 05/08/17 MF BC TSh DP				
WBS ID	Task	Ref. person @Elettra (mails below)	Ref. Person @ ESS	mails (externals)	NOTES	
11.7.7.1	General issues, mngt. & admins	Mario	Benjamin, Tom & Daniel	benjamin.cheymol@esss.se, thomas.shea@esss.se, Daniel.PisoFernandez@esss.se	Diags and ICS	
11.7.7.2	Analog Front End (AFE), SEM	Raffaele	Benjamin			
11.7.7.3	Optical Front End (OFE), Scintillator	Sandi	Benjamin			
11.7.7.3.1	Back End (BE), SEM & Scintillator	Raffaele	Hinko	hinko.kocevar@esss.se		
11.7.7.4	Interfacing to MPS	Sandi	Szandra, Julen	Szandra.Kovecses@esss.se, JulenEtxeberria.Malkorra@esss.se		
11.7.7.5	Motion Controllers	Sandi	Julen, Thomas, Torsten	Thomas.Gahl@esss.se torsten.bogershausen@esss.se		
11.7.7.6	Mech Integration	Mario	Nick Gazis	nick.gazis@esss.se	integration in the tunnel (FE?)	
11.7.7.6.1	Interfacing to ESS Bilbao Mechanics	Mario	Ibon, Ben, Alvaro	ibustinduy@essbilbao.org, avizcaino@essbilbao.org		
11.7.7.6.2	Interfacing to Dan Physic Mechanics	Mario	Ben			
11.7.7.7	Cabling (connectors and cables)	Sandi	Lia	Evangelia.Vaena@esss.se		
11.7.7.7.1	Cabling (on-board rack)	Sandi	Edvard	Edvard.Bergman@esss.se		
11.7.7.8	ICS WS integration	Stefano	Hinko, Julen			
11.7.7.8.1	ICS WS integration (low level)	Stefano	Hinko, Han	han.lee@esss.se	uTCA ADCs CPUs	
11.7.7.8.1	ICS WS integration (motion controller)	Stefano	Torsten, Anders	Anders.Sandstrom@esss.se	etherCAT	
11.7.7.8.2	ICS WS integration (graphic panel)	Stefano	Ben, Han		engineering and operator	
11.7.7.8.3	ICS WS integration (computation)	Stefano	Ben, Han			
11.7.7.8.4	<i>Timing</i> (event system)	Stefano	Timo K.	Timo.Korhonen@esss.se	synchronization issues	
11.7.7.9	Handover	Mario	Ben		from ST to ESS ERIC	
11.7.7.9.1	Test at Partner Lab. (SACLAY)	Mario	Ben			
11.7.7.9.2	Shipment and delivery	Mario	Hinko, Clement	clement.derrez@esss.se	send and receive, where, when	
11.7.7.9.3	On site ESS commissioning	Raffaele	Ben, Hinko			
11.7.7.9.4	Installation	Sandi	Clement			





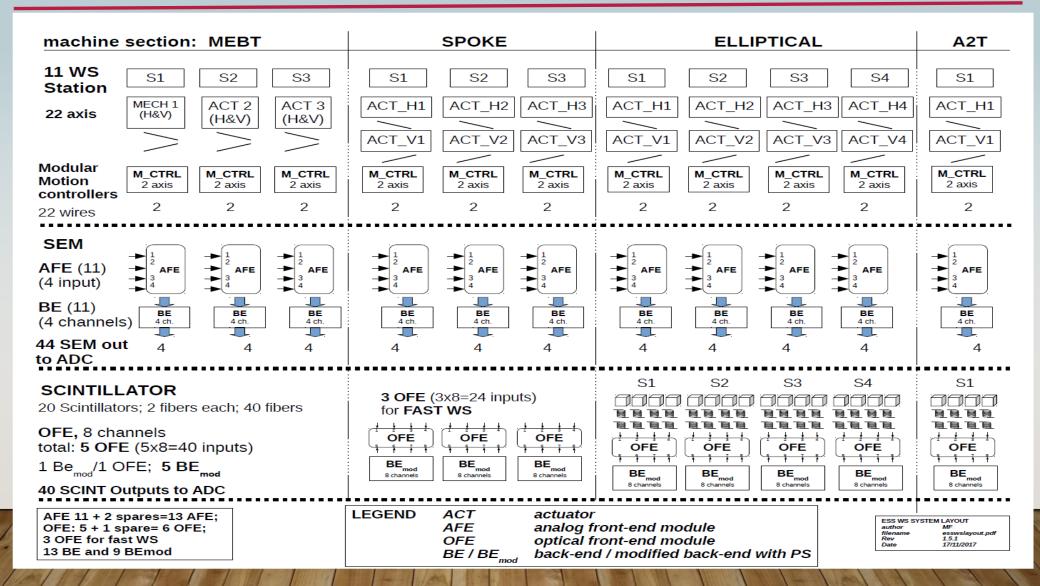
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SOURCE

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## (LOW LEVEL) LAYOUT OF THE WS ACQ SYS





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TASK % DONE	E /	LEFT TO DO
Design (HW & SW)	95%	BE <sub>mod</sub> ; 100% by CDR
PDR-1 & PDR-2	100%	28 Jun 2016 & 13 Dec 2016
Prototyping HW	90%	Be <sub>mod</sub> / 2 <sup>nd</sup> proto production
Prototyping SW	70%	synch data storage on EPICS
		transverse prof. reconstruction
HW integration into ICS	90%	OFE interfacing to µ-TCA
Laboratory test (no beam)	80%	transverse prof. reconstruction
<b>Test with beam</b> (AFE + BE)	<b>50%</b>	tested on LINAC 4 @ CERN
CDR-I & CDR-2	30%	due by 16 Feb 2018
Vertical integration @ ESS	20%	due by 18 May 2018





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5	TASK % DONE	/	LEFT TO DO
٠	SEM series production	0%	Feb-Jun 2018
•	I <sup>st</sup> SEM batch delivery	0%	due by 20 Jul 2018 (MEBT WS)
•	TRR	0%	due by 14 Sep 2018
•	SAR-I: SEM series test in Lab	0%	due by 12 Oct 2018
•	Start MEBT installation	0%	due by 15 Nov 2018
•	MEBT beam commissioning	0%	15 Jan 2019
	SCINT series production I <sup>st</sup> SCINT batch delivery	0% 0%	May-Oct 2018 due by 10 Dec 2018 (ELLIPT. WS)
	SAR-2: SCINT series test in Lab	0%	due by 11 Jan 2019
	End of Installation	0%	I Jun 2020



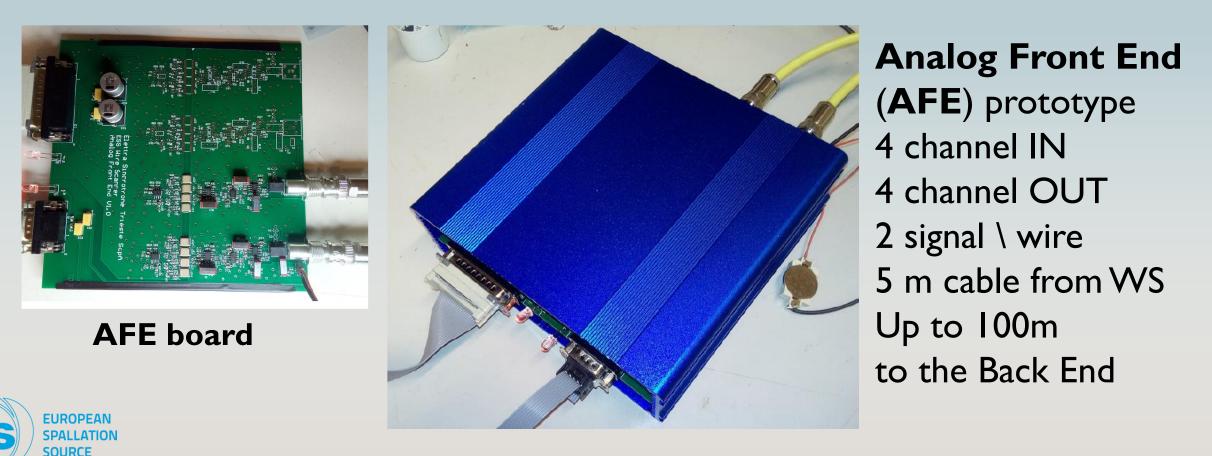


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### **ACHIEVEMENTS TO DATE - SEM**



**ALL DETAILS AND MUCH MORE IN RAFFAELE'S TALK** 



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**ACHIEVEMENTS TO DATE - SEM** 

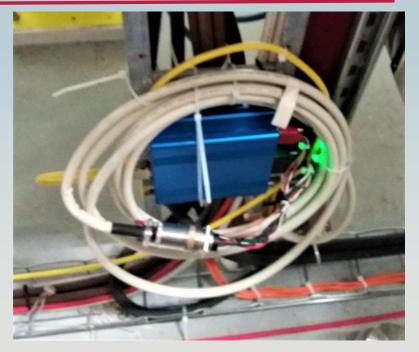
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### Elettra Team during WS ACQ SYS installation on LINAC4 at CERN







The complete WS ACQ system has been moved and installed on LINAC4: µ-TCA and VME crates + **Back End Analog Front End** in LINAC tunnel



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**ACHIEVEMENTS TO DATE - SEM** 

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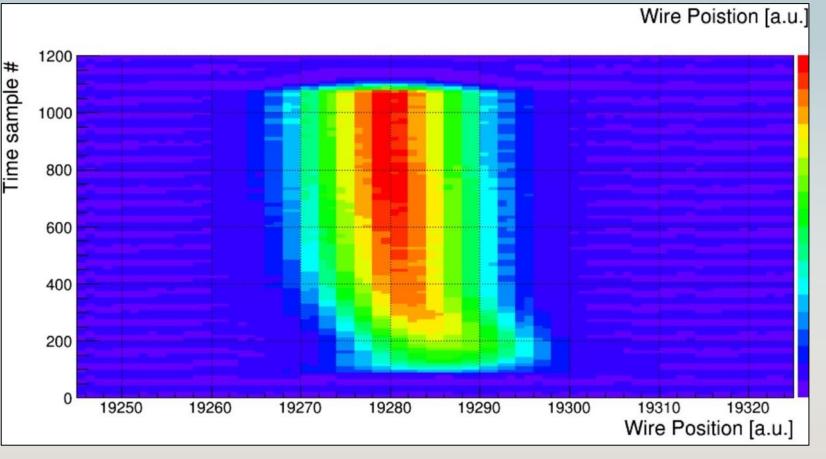
# PLOT of wire scanner acquired data

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100µs long macropulse LINAC4 trigger at 1Hz ADC board at 10MSPS (up to 125MSPS)

Merging of HIGH GAIN & LOW GAIN data





#### **COURTESY OF FEDERICO RONCAROLO AT CERN**



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### ACHIEVEMENTS TO DATE - SEM

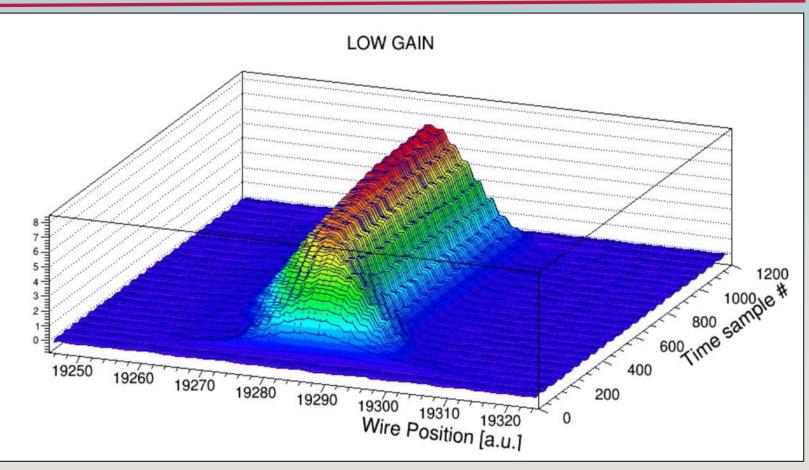
**3-D PLOT of wire scanner acquired data** (vertical profiles)

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The high speed (up to 125MSPS) ADC board allows the bunch tomography which could useful in LINAC tuning (low losses)

Also, the high speed ADC will be most useful for ESS  $5\mu$ sec bunch acquisition

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## ACHIEVEMENTS TO DATE - SCINT



**Optical Front End** (**OFE**) prototype 8 channel IN 8 channel OUT 2 signal \ SCINT 4 SCINT \WS FO from WS to OFE Up to 150m Modified Back End (BE<sub>mod</sub>)

### ALL DETAILS AND MUCH MORE IN SANDI'S TALK



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-0.00216558

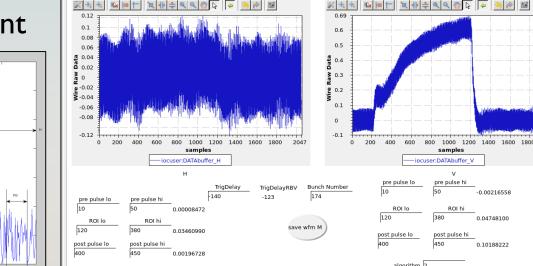
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ACHIEVEMENTS TO DATE - SW

ESS development environment: set-up and running Both µ-TCA (CPU, ADC, Ev\_Rx) and VME (Ev\_Gen) systems running Acquisition FW done Control Panels: prototype running Successfully field tested at CERN WS IN channels markers beam motion Back End simul Profile processing algorithm: under development Synchronous data storage: under development





### **COURTESY OF STEFANO**



# NEXT STEPS – OPEN ISSUES



Need a strong joint commitment to the bi-lateral ESS-ST Contract signature
>> it will un-lock resources at ST, enabling series production in 2018
CDR-1 & CDR-2 milestone in early 2018 (Jan/Feb)
Careful cables, cabling and installation (racks) double check (RUNNING!)
Vertical integration tests (mid 2018, the latest):

- > wire scanner mechanics to motion controller and acquisition system
- >WS acquisition system interfacing to ESS ICS and timing
- >WSACQ SYS interfacing to MPS
- Delivery and **in-house acceptance** procedure (what, where and when) In-situ WS ACQ SYS installation infrastructure set-up (1 by 1 WS stations)

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Thank you for your attention

