Experiences on J-PARC LINAC LLRF Systems



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Contents

- 1 Introduction
- 2 Reference timing system
- 3 Digital feedback system
- 4 Beam compensation system
- 5 Auto-tuning and auto-startup process
- 6 Summary

1 Introduction

J-PARC LINAC



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J-PARC LINAC





J-PARC LINAC



J-PARC LINAC LLRF system



Block diagram of J-PARC LINAC LLRF



Basic requirements of J-PARC LINAC LLRF:

- > Stabilities of rf field: \pm 1% in amplitude and \pm 1° in phase.
- > Auto-tuning of rf cavity.
- Interlock system.
- > Operation system with a great convenience, high reliability, and fast response.

2 Reference timing system

New master oscillator for LO signals
 LO signal distribution system
 12MHz reference distribution system

1) New master oscillator for LO signals





2) LO signal distribution system



The LO signals are optically amplified and divided into 17/16 lines, then furthermore divided into 5: one of them is returned to the front end for phase monitor; the others will be used for the LLRF systems at each station.

The phase instability by monitoring the returned signals is about ±0.2 deg., better than requirements (±0.3 deg).
¹¹

3) 12MHz reference distribution system

New system using optical couplers



New system using optical coupler



Jitter between LO and 12MHz reference signals reduced from **315ps** to **30ps**.

13

3 Digital feedback system

- 1) Feedback control circuits
- 2) Improvements of analog devices
- 3) Digital functions idealizing driving source
- 4) Optimization of feedback parameter setting

1) Feedback control circuits



2) Improvements of analog devices



Mixer&IQ board

Introducing a **temperaturecompensation attenuator** into the output circuits.



Temperature coefficient of amplitude of the down-converter output signal



Using **temperature-compensation capacitors** in the Low-Pass Filter (LPF) of the LO output circuits.





Temperature coefficient of phase of the LO output signal

3) Digital functions idealizing driving source



(1) IQ offset compensation



IQ modulator output at SDTL13 with or without IQ offset compensation.

(2) Automatic sag compensation



Feedforward tables:

$$FF _ I _ t = A _ t \times \left[1 - \Delta \alpha \left(t - \frac{t_1 + t_2}{2}\right)\right] \cdot \cos\left[\theta - \Delta \phi \left(t - \frac{t_1 + t_2}{2}\right)\right]$$
$$FF _ Q _ t = A _ t \times \left[1 - \Delta \alpha \left(t - \frac{t_1 + t_2}{2}\right)\right] \cdot \sin\left[\theta - \Delta \phi \left(t - \frac{t_1 + t_2}{2}\right)\right]$$
20

(3) Non-linearity compensation of klystron input-output



4) Optimization of feedback parameter setting

(1) Feedback gain gradually increased



Overshot and deformation of RF waveforms minimized. Smooth RF waveforms obtained with feedback ON, especially during the rising time in the pulse.

(2) FF_BASE and FB_REF tables optimized



RF waveforms of both of the DAC and ADC **not changed much** between FB_OFF and FB_ON.

A long flat top obtained with a good stability of feedback system.

4 Beam compensation system

Automatic beam loading switching
 Automatic FF_beam setting
 Chopped beam compensation
 Performances

1) Automatic beam loading switching



- Add a mode-exchanging signal (FF_Beam_Mult gate), detected by the FPGA.
- In the FPGA program, the different value of FF_beam will be applied corresponding to its pulse width.

Switching the beam loading compensation could be realized in real time before beam coming. 25

2) Automatic FF_beam setting

Using DAC information before beam and in beam:

 $AMP_beam = (I_beam^2 + Q_beam^2)^{0.5}$ $PHA_beam = atan2(I_beam, Q_beam) \times 180/3.1416$ to obtain FF_beam: AMP FF beam = AMP beam / DAC amp calibr

PHA_FF_beam= PHA_beam-DAC_pha_calibr



3) Chopped beam compensation

At J-PARC, chopped beam is accelerated after chopper station. Chopped beam compensation is carried out.



Chopping signal and timing of the LLRF system.

- Add chopping signal and beam_gate, detected by the FPGA.
- In the FPGA program, the FF_beam is fed forward when the logical AND with inputs of the beam gate and chopping signal has the value 1.

4) Performances

Stabilities of amplitude and phase without/with beam operation

Without beam	324MHz RF Cavities	972MHz RF Cavities			
∆A _(p-p) / A	~ ±0.12%	~ ±0.12%			
$\Delta \phi_{(p-p)}$	$\sim \pm 0.08^{\circ}$	$\sim \pm 0.11^{\circ}$			
16mA chopped-beam	324MHz RF Cavities	972MHz RF Cavities			
∆A _(p-p) / A	~ ±0.14%	~ ±0.27%			
Δφ _(p-p)	~ ±0.08°	~ ±0.16°			
30mA chopped-beam	324MHz RF Cavities	972MHz RF Cavities			
30mA chopped-beam ∆A _(p-p) / A	324MHz RF Cavities ±0.12%~±0.31%	972MHz RF Cavities ~±0.45%			
30mA chopped-beam ΔA _(p-p) / A Δφ _(p-p)	324MHz RF Cavities $\pm 0.12\% \sim \pm 0.31\%$ $\pm 0.09^{\circ} \sim \pm 0.14^{\circ}$	972MHz RF Cavities ~±0.45% ~±0.19°			
30mA chopped-beam ΔA _(p-p) / A Δφ _(p-p)	324MHz RF Cavities $\pm 0.12\% \sim \pm 0.31\%$ $\pm 0.09^{\circ} \sim \pm 0.14^{\circ}$	972MHz RF Cavities ~±0.45% ~±0.19°			
30mA chopped-beam ΔA _(p-p) / A Δφ _(p-p) 50mA chopped-beam	324MHz RF Cavities ±0.12%~±0.31% ±0.09°~±0.14° 324MHz RF Cavities	972MHz RF Cavities ~±0.45% ~±0.19° 972MHz RF Cavities			
30mA chopped-beam $\Delta A_{(p-p)} / A$ $\Delta \phi_{(p-p)}$ 50mA chopped-beam $\Delta A_{(p-p)} / A$	324MHz RF Cavities ±0.12%~±0.31% ±0.09°~±0.14° 324MHz RF Cavities ±0.18%~±0.69%	972MHz RF Cavities ~±0.45% ~±0.19° 972MHz RF Cavities ~±0.94%			

5 Auto-tuning and auto-startup process

- 1) The first generation
- 2) The second generation
- 3) The third generation
- 4) Performances

(2006.10 - 2009.09)1) The first generation

80

Time (s)

Time (us)

100 120 140 160

end of

RF pulse

phase

slope

When RF power feeds to a cavity, cavity temperature will increase, and its resonance frequency will change. Auto-tuning system is very important for accelerator operation, especially during cavity warm-up.

The *first generation* of auto-startup process:

using a mechanical tuner controller by DSP.



2) The second generation^(2009.10-2013.11)

For cavity warm-up process, instead of using mechanical tuner controller, the *second generation* of auto-startup process:

using input RF frequency tuning by FPGA.



Important advantages:

- We can <u>restart RF operation very quickly</u>, since now it's <u>not necessary to move</u> the tuner from "hot position" back to "cold position".
- It also provides the tuner with <u>a good protection</u> from damage due to frequent movements.
- Now, RF power can be fed to RF cavity more <u>smoothly</u> and <u>quickly</u>: <u>Very good matching</u> maintained between RF input and RF cavity in real-time, <u>Time for RF startup</u> reduced.

3) The third generation

The third-generation of a novel auto-startup process:

<u>using input RF frequency tuning + mechanical tuner controller.</u>



Two *most important advantages*:

- <u>Time for cavity start-up process</u> will be <u>shortened</u> furthermore;
- <u>A "perfect" matching</u> between RF source and RF cavity will be <u>obtained</u> during entire RF operation.

(2013.12-now)

4) Performances

Trend data during RF startup process using the third generation



Movie for RF startup process using the third generation

- In the actual operation, it took about 1.5 min to recover RF fields in RF cavities ready for beam acceleration even after a long-term shut down.
- Recently, the start-up time was reduced furthermore to about 20 seconds for all cavities.

Movie for RF start-up

In our operation system, for RF start-up, we only need to push one button:



RF waveform during RF start-up process



6 Summary

 1) Experiences and performances of J-PARC LINAC LLRF systems
 2) Interface of LLRF operation system
 3) Consideration for future
 4) Spare information

1) Experiences and performances of J-PARC LINAC LLRF systems

Improvements and experiences on J-PARC LINAC LLRF:

Reference timing system Digital feedback system Beam compensation system Auto-tuning and auto-startup process

Excellent performances :

- Very good RF field stabilities are obtained with beam operation.
 - <u>A novel auto-startup process</u> is available with "perfect" matching between RF source and RF cavity during entire RF operation.

An RF operation system is achieved with great convenience, high reliability, and fast response.

2) Interface of LLRF operation system

(1) All stations

HVDC Locate Remote Status Target Status Run Run LV-READY LV-ON LV-ON Cathode HV-READY HV-ON HV-ON HV-O	KLYSTRON LLRF AMP I/L Locate Status RF-ON TANK1 TANK2 PaRFQ PaRFQ Remote Run 4006 3999 PaBUN1 Remote Run 3998 0 PaBUN2 Remote Run 2 3999 PaCHOP1 Remote Run 4026 4028 PaCHOP2 Remote Run 3986 3987 PaDTL2 PaDTL2 Run 3998 4002 PaDTL3 PaDTL3 Remote Run 4000 3998	HVDC DHVDC07 Locate PS ON I// Status Target Status LV-READY I// Run Run HV-READY I// Run Run HV-READY I// ALL Volt. 106.17 kV VCB-ON I// DHVDC08 Locate PS ON I// Status Target Status LV-ON I// Status Target Status HV-READY I// Run Run HV-READY I// Cathode PS ON I// I// Cathode PULSE-READY I// I// Run Run HV-READY I// Run Run PULSE-READY I// ALL Volt. 104.18 kV VCB-ON I//	KLYSTRON LLLRF L Locate L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L L	AHP Status RF-0N TANK1 Run 2295 2297 Run 3993 4002 Run 3993 4002 Run 4002 3998 Run 4002 3997 Run 3993 4002 Run 4002 3997 Run 3993 4008 Run 3993 3996 Run 3993 3999
Locate PS ON Remote LV-READY Status Target Status Run Run Run HV-READY Cathode PULSE-READY ALL Volt. 88.56	P2S01 P2S01 Remote Run 4000 3998 P2S02 P2S02 Remote Run 4000 3998 P2S03 P2S03 Remote Run 4000 3998 P2S04 P2S04 Remote Run 4000 3999	DHVDC09 Locate PS ON Remote LV-READY Status Target Status HV-READY Run Run HV-ON Cathode PULSE-READY ALL Volt. 103.22 kV VCB-ON	DateD	Run 4000 4000 Run 3998 4002 Stop 16 6 Run 3997 4003
CHVDC03 Locate PS ON Remote LV-READY Status Target Status HV-READY Run Run HV-ON Cathode PULSE-READY ALL Volt. 100.86 kV VCB-ON	P3S05 PaS05 Remote Run 3999 4000 P3S06 P3S06 Remote Run 3996 4001 P3S07 P3S07 Remote Run 4000 3997 P3S08 P3S08 Remote Run 4000 4001	DHVDC10 Locate PS ON Remote LV-READY Status Target Status LV-ON Run Run HV-READY Cathode PULSE-READY ALL Volt. 101.98 kV VCB-ON	DacS13DacS13RemoteDacS14DacS14RemoteDacS15DacS15RemoteDacS16DacS16Remote	Run40013997Run39934006Run40093991Run39964005
CHVDC04 Locate PS ON Remote LV-READY Status Target Status HV-READY Run Run HV-ON Cathode PULSE-READY ALL Volt. 103.11 kV VCB-ON	P3S09 P3S09 Remote Run 3999 4002 P3S10 P3S10 Remote Run 3999 4003 P3S11 P3S11 Remote Run 4001 3998 P3S12 P3S12 Remote Run 3997 4001	DHVDC11 Locate PS ON Remote LV-READY Status Target Status LV-ON Run Run HV-READY Cathode PULSE-READY ALL Volt. 103.32 kV VCB-ON	DacS17DacS17RemoteDacS18DacS18RemoteDacS19DacS19RemoteDacS20DacS20Remote	Run 3991 4008 Run 3999 4001 Run 4005 3993 Run 4005 3981
CHVDC05 Locate PS ON Remote LV-READY Status Target Status HV-READY Run Run HV-ON Cathode PULSE-READY ALL Volt. 105.41 kV VCB-ON	DyS13 DyS13 Remote Run 4002 3998 DyS14 DyS14 Remote Run 3995 4004 DyS15 DyS15 Remote Run 4002 3998 DyS14 DyS15 Remote Run 4002 3998 DyS16 DyS16 Remote Run 3997 4001	DHVDC12 Locate PS ON Remote LV-READY LV-ON Status Target Status HV-READY Run Run HV-ON Cathode PULSE-READY ALL Volt. 99.78 kV VCB-ON	DEACS21 DIBIN1 Remote	Run 3995 4003
CHVDCO6 Locate PS ON Remote LV-READY Status Target Status HV-READY Run Run HV-ON Cathode PULSE-READY ALL Volt, 82.14 kV VCR-ON	D DBUN3 Remote Run 4003 3997 D DBUN4 DBUN4 Remote Run 4002 3999		QDBUN2 QDBUN2 Remote	Run 4002 3996

(2) DTL01 LLRF

		FB AMP Value	4000	4000	SET Correc	∶t. FPGA AMP	1046	1046 SET	Tuner1 Sensitivit	y 200,00 0.00 SET
LI_DTL1:LLRF01	FB	REF Phase Value	60.0	60.0	SET Correct.	. FPGA Phase	106.0	106.0 SET	Tuner1 Detunin	19 0.00 0.00 SET
		FF AMP Value	0	0	SET	FF-Vall AMP	0		- Tuner2 Sensitivit	y 0.00 0.00 SET
	GO-STOP FF B	EAM Phase Value	0.0	0.0	SET FF	-Vall Phase	0.0		Tuner2 Detunin	19 0.00 0.00 SET
Location Status larget Status Remote DIN DIN	CO-PLIN T	P Value	70	b	SET	FE-Val2 AMP	1000	D SET	Tank1 Delta-	-f 0.70 0.00 SET
Kelloce Koll Koll		I Value	80	þ h	SET FE	-Val2 Phase	180.0	D D SET	Tank2 Delta-	-f 0.70 0.00 SET
	KESET	DI Dice Time	100	<u>м</u>	CET I	FE_U-17 OME	· 100.10		L f_Panao Tim	10 0.10 0.00 <u>SET</u>
LLRF Control	1	FI KISE IIME	100	۲ <u>ــــــــــــــــــــــــــــــــــــ</u>	SET E		230		T-Kange III	
DCPCI 2 CTL RF ON/OFF	ON OFF	FB Start	5	<u>p</u>	SET FF	-Val3 Phase	: 35.0	p.o SET		e 5p <u>SET</u>
EDSLOW ST CTL FB ON/OFF	ON OFF	FB Stop	1023	p .	SET	FF-Val4 AMP	420	p <u>SET</u>	Freq Shift Timeu	_P 120 μ <u>SET</u>
FF Beam UN/UFF FF Beam UN/UFF FF Beam UN/UFF		FB Limit	8191		FF	-Val4 Phase	45.0	0.0 <u>SET</u>	Detuning Delta-f	1 0.0 0.0 <u>SET</u>
REMOTE/LOCAL		Loop Delay	0	þ j	SET	FF-Val5 AMP	1740	0 SET	📔 Decay Start Tim	e 10 <u>SET</u>
LOPHHSE MUN Reset		T Wave Rising	20	þ	SET FF	-Val5 Phase	28.0	0.0 SET	📔 🛛 Decay Interva	1 10 0 SET
SlowST ON/OFF		I Offset	-109	-109	SET	CHOP ON	1	0 1 SET	QR Reboot Tim	ie 2.0 0.0 <u>SET</u>
AutoRec ON/OFF	ON OFF	Q Offset	-116	-116	SET	CHOP Delay	150	0 SET	QR Moniter Tim	e 1 SET
SlowST ON Freq shift //Mecha Tun	Shift Tuner Sag	Correction AMP	10.7	10.7	SET	Tuner Start	1.0	0.0 SET	QR Count Tim	e 5 0 SET
SlowST OFF:Freq shift //Mecha Tun	Shift Tuner Sag C	orrection Phase	18.3	18.3	SET	Tuner Stop	0.5	0.0 SET	Beam Gate Dela	xy 36 0 SET
Analb UN/UFF	EB1 EB2 Corr	ection CAV1 AMP		984	SET Sar	Delina Point	425	h SET	i	· · · · · · · · · · · · · · · · · · ·
Phase Diff /Phase Dec	Diff Decay Corren	tion CAV1 Phase	51.0	51 0	CET 1	st Sten Rate			1	D ILK Count
Arb Freq 📕 /Random Freq 📕	Arb Randm Conn	cotion CAU2 AMP	1100	1400 k		ODCZ limit	0101		1	
CHOP PHA Reverse ON/OFF		ection thvz HMP	07.4	µ108	SET	ADCS LIMIT	0131		1	
CHOP PHA Reverse: MediumP /MacroP	Lorrec	tion LHV2 Phase	93.4	93.4	SET	HUC4 Limit	8191	p <u>SET</u>	1	
HUL Monitor UN/UFF L ADC Comparison SET	SET	tion Input1 AMP	1372	1372	SET Limi	t MUN Start	. 0	p <u>SET</u>	1	
FF Sag ON/OFF	ON OFF Correcti	on Input1 Phase	51,5	51.5	SET Lin	nit MON Stop	1023	<u>p</u> SET		KLY Arc Sensor
	Correc	tion Input2 AMP	1382	1382	SET	T Sag Ref	425	D SET		TANK1 Arc Sensor
	Correcti	on Input2 Phase	282,2	282.2	SET	T FF Rising	20	<u>)</u> SET]	TANK2 Arc Sensor
						T FB Rising	40	0 SET	1	Pf Level Alarm V1
cPCI DAC Status					_	Tk1	Tk2			Pf Level Alarm V2
ADC3 Limit OK			IN TEMP	OUT TEMP	I	k 990	1000			Pb Level Alarm V1
ADC4 Limit OK		Circulator	27.8	28.0		PF	Pr			Pb Level Alarm V2
DAC Limit OK		Dummy Road	28.0	27.6	V	1 1180	70		ILK	Pb Level Alarm V3
FPGA Limit OK		24Mild House	TUNER1	TUNER2	v u	z 510	20	PPS RF I		
Chop Gate Sig. Monitor OK		Position	38,60	53.65	· ·	J JIV				
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FF Beam 03 Sig. Monitor OK		Cold POS	28,96	54.03		18,96	18,93	I	Gate Alarm 📃 📃	ADC4Limit
FF Beam 04 Sig. Monitor OK	Turier commu₊ scacus	U-+ DOC	75 CO	54 03	-		-0.07		KLY PS OK 📃 📃	DAC Limit
··· ··································	cPCI Commu.Status	HOT PUS	33,00	04400	Delta-	F -0.08	×+×1			
	cPCI Commu.Status 🗌	Origin	90,00	45,00	Delta- Delta-Pk	F -0.08 y -0.59	-0,49	TANK1 AND I	Contact OK	PU OF
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Tuner Control Register CAV1 CAV2 Emergency Stop Drive Error Motor OverHeat PO entry Alarm	cPCI Commu.Status	Hot FUS Origin cPCI Req. POS	90,00 38,59 Vc1 Phs1	45.00 54.03 FBM Tank 3997 59.9	Delta- Delta-PH CA' VAC 1 ADC	F -0.08 ng -0.59 /1 5 Ci .79 AMP 1 3999	-0,49 AV2 8 0,02 Phase 59,9	TANK1 AND C TANK2 AND C TANK1 V TANK1 V TANK2 V Circul Dummy	Contact OK	FPGA Limit PLL OK FB Temp. Error Cir. Temp.Dif Error Trombone Error
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Tuner Control Register CAV1 CAV2 Emergency Stop Drive Error Motor OverHeat PO entry Alarm IN Limit OUT Limit Hi Monitor Lo Monitor	cPCI Commu. Status	Hot PUS Origin cPCI Req. POS	90.00 38.59 Vc1 Phs1 Vc2 Phs2 Slow No.	45.00 54.03 FBM Tank 3997 59.9 4001 59.9 0	Delta- Delta-PH CA' VAC 1 ADC ADC ADC ADC	F -0.08 y -0.59 /1 5 Ci AMP 1 3999 2 4005 3 4004 4 3994 4 3994	-0.49 AV2 8 0.02 8 Phase 59.9 59.9 60.1 60.2	TANK1 AND G TANK2 AND C TANK1 W TANK2 W Circul Dummy F 50W Amp P 50W Amp T 50W Amp T	Contact OK	FPGA Limit PLL OK FB Temp. Error Cir. Temp.Dif Error Trombone Error Drive Error 1-1 IN LIMIT 1-1 OUT LIMIT 1-1 MOTOR OVERHEAT1-1
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Tuner Control Register CAV1 CAV2 Emergency Stop Drive Error Motor OverHeat PO entry Alarm IN Limit OUT Limit Hi Monitor Lo Monitor Driving Tuner Driving Tuner	cPCI Commu. Status Mask Status1 00 Mask Status2 63 Mask Status3 00 Mask Status4 00 Mask Status5 00 Mask Status5 00	RF Drigin cPCI Req. POS RF Trom	90,00 38,59 Vc1 Phs1 Vc2 Phs2 Slow No, Off Time bone POS RR Count	45.00 54.03 FBM Tank 3997 59.9 4001 59.9 0 685 0,1	Delta- Delta-PH CAV VAC 1 ADC ADC ADC DA ADC1(t=C ADC1(SF ADC1(t=C	F -0.08 y -0.59 /1 5 Ci AMP 1 3999 2 4005 3 4004 3 4004 3 4004 4 3994 1 3994 1 3994 0 4152 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	-0.49 AV2 8 Phase 59.9 59.9 60.1 60.2 167.2 0.0 0.0	TANK1 AND C TANK2 AND C TANK1 W TANK2 W Circul Dummy F 50W Amp P 50W Amp T 50W Amp T 50W Amp Out U 50W Amp Out U 50W Amp Out L S0W Amp Out L	Contact OK	PPGA Limit PLL OK FB Temp. Error Cir. Temp.Dif Error Trombone Error Drive Error 1-1 IN LIMIT 1-1 OUT LIMIT 1-1 Drive Error 1-2 IN LIMIT 1-2 OUT LIMIT 1-2 OUT LIMIT 1-2 OUT LIMIT 1-2 OUT LIMIT 1-2

3) Consideration for future

Organize and refine each job and process for automation, for example, RF calibration and beam compensation with environment changing (drifted HVDC, variated beam, ...)

LLRF is one of the most interesting jobs. Never stop in approaching a simple-and-perfect control system.

Upgrade the LLRF system by using MTCA.4.

4) Spare information

Update: 2018/01/09

	Units for	Units for spare							
LLRF	operation	CPU	Ю	DSP- FPGA	Mix-IQ	RF	VS- Meter	Pre-amp	
324MHz	24(+1)	C	Л	Δ	4	12	3	1	
972MHz	25	0	4	4	9	7	2	2	

Klystron	Units for operation	Units for spare
324MHz	20	6
972MHz	25	5 (+2, next month)

Thank you very much for your attention !